A T-Connected Transformer and Three-leg VSC Based DSTATCOM for Power Quality Improvement

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***Abstract*—In this paper, a new three-phase four-wire distribution static compensator (DSTATCOM) based on a T-connected transformer and a three-leg voltage source converter (VSC) is proposed for power quality improvement. The T-connected transformer connection mitigates the neutral current and the three-leg VSC compensates harmonic current, reactive power, and balances the load. Two single-phase transformers are connected in T-configuration for interfacing to a three-phase four-wire power distribution system and the required rating of the VSC is reduced. The insulated gate bipolar transistor (IGBT) based VSC is supported by a capacitor and is controlled for the required compensation of the load current. The dc bus voltage of the VSC is regulated during varying load conditions. The DSTATCOM is tested for power factor correction and voltage regulation along with neutral current compensation, harmonic elimination, and balancing of linear loads as well as nonlinear loads. The performance of the three-phase four-wire DSTATCOM is validated using MATLAB software with its Simulink and power system blockset toolboxes.**

***Index Terms*—Distribution static compensator (DSTATCOM), neutral current compensation, power quality improvement, T-connected transformer, voltage source converter (VSC).**

I. Introduction

THREE-PHASE four-wire distribution systems are facing severe power quality problems such as poor voltage regulation, high reactive power and harmonics current burden, load unbalancing, excessive neutral current, etc. [1]–[5]. Three-phase four-wire distribution systems are used in commercial buildings, office buildings, hospitals, etc. Most of the loads in these locations are nonlinear loads and are mostly unbalanced loads in the distribution system. This creates excessive neutral current both of fundamental and harmonic frequency, and the neutral conductor gets overloaded. The voltage regulation is also poor in the distribution system due to the unplanned expansion and the installation of different types of loads in the existing distribution system. In order to control the power quality problems, many standards are proposed, such as the IEEE-519 standard [6].

There are mitigation techniques for power quality problems in the distribution system and the group of devices is known by the generic name of custom power devices (CPDs) [1]. The distribution static compensator (DSTATCOM) is a shunt-connected CPD capable of compensating power quality problems in the load current. Some of the topologies of DSTATCOM for three-phase four-wire system for the mitigation of neutral current along with power quality compensation in the source current are four-leg voltage source converter (VSC), three single-phase VSCs, three-leg VSC with split capacitors [3], three-leg VSC with zig-zag transformer [7]–[9], and three-leg VSC with neutral terminal at the positive or negative of dc bus [10]. The voltage regulation in the distribution feeder is improved by installing a shunt compensator [11]. There are many control schemes reported in the literature for control of shunt active compensators such as instantaneous reactive power theory, power balance theory, synchronous reference frame theory, symmetrical components based, etc. [12], [13]. The synchronous reference frame theory [12] is used for the control of the proposed DSTATCOM.

In this paper, a new topology of DSTATCOM is proposed for a three-phase four-wire distribution system, which is based on three-leg VSC and a T-connected transformer. The T-connected transformer is used in the three-phase distribution system for different applications [14]–[16]. But the application of T-connected transformer for neutral current compensation is demonstrated for the first time. Moreover, the T-connected transformer is suitably designed for magnetic motive force (mmf) balance. The T-connected transformer mitigates the neutral current and the three-leg VSC compensates the harmonic current and reactive power, and balances the load. The insulated gate bipolar transistor (IGBT) based VSC is self-supported with a dc bus capacitor and is controlled for the required compensation of the load current. The DSTATCOM is designed and simulated using MATLAB software with its Simulink and power system blockset (PSB) toolboxes for power factor correction and voltage regulation along with neutral current compensation, harmonic elimination, and load balancing with linear loads as well as nonlinear loads.

II. System Configuration and Design

Fig. 1(a) shows the single-line diagram of the shunt-connected DSTATCOM-based distribution system. The dc capacitor connected at the dc bus of the converter acts as an energy buffer and establishes a dc voltage for the normal operation of the DSTATCOM system. The DSTATCOM can be operated for reactive power compensation for power factor correction or voltage regulation. Fig. 1(b) shows the phasor diagram for the unity power

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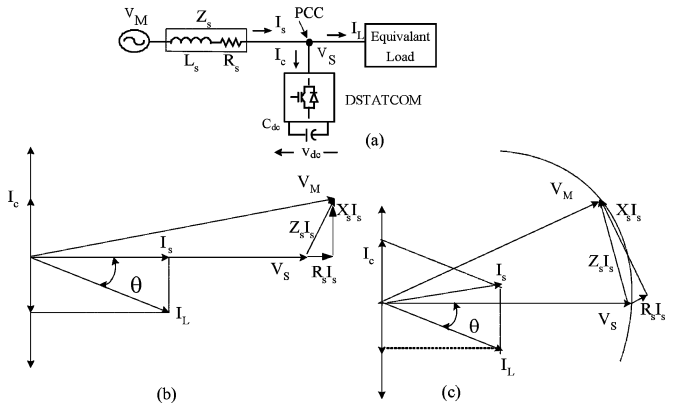

Fig. 1. (a) Single-line diagram of DSTATCOM system. (b) Phasor diagram for UPF operation. (c) ZVR operation.

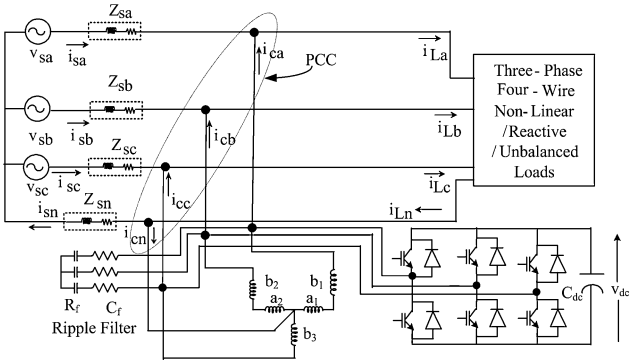

Fig. 2. Schematics of the proposed three-leg VSC with T-connected-transformer-based DSTATCOM connected in distribution system.

factor operation. The DSTATCOM injects a current I_c such that the source current is only I_s, and this is in-phase with voltage. The voltage regulation operation of DSTATCOM is depicted in the phasor diagram of Fig. 1(b). The DSTATCOM injects a current I_c such that the voltage at the load (V_S) is equal to the source voltage (V_M).

The proposed DSTATCOM consisting of a three-leg VSC and a T-connected transformer is shown in Fig. 2, where the T-connected transformer is responsible for neutral current compensation. The windings of the T-connected transformer are designed such that the mmf is balanced properly in the transformer.

A three-leg VSC is used as an active shunt compensator along with a T-connected transformer, as shown in Fig. 2, and this topology has six IGBTs, three ac inductors, and one dc capacitor. The required compensation to be provided by the DSTATCOM decides the rating of the VSC components. The data of DSTATCOM system considered for analysis is shown in the Appendix. The VSC is designed for compensating a reactive power of 12 kvar, as decided from the load details. The selection of interfacing inductor, dc capacitor, and the ripple filter are given in the following sections.

A. DC Capacitor Voltage

The minimum dc bus voltage of VSC of DSTATCOM should be greater than twice the peak of the phase voltage of the system [17]. The dc bus voltage is calculated as

$$V_{\rm dc} = \frac{2\sqrt{2}V_{LL}}{\sqrt{3}m} \tag{1}$$

where m is the modulation index and is considered as 1, and V_{LL} is the ac line output voltage of DSTATCOM. Thus, $V_{\rm dc}$ is obtained as 677.69 V for V_{LL} of 415 V and is selected as 700 V.

B. DC Bus Capacitor

The value of dc capacitor ($C_{\rm dc}$) of VSC of DSTATCOM depends on the instantaneous energy available to the DSTATCOM during transients [17]. The principle of energy conservation is applied as

$$\frac{1}{2}C_{\rm dc}[(V_{\rm dc}^2) - (V_{\rm dc1}^2)] = 3V\,(aI)\,t \tag{2}$$

where $V_{\rm dc}$ is the reference dc voltage and $V_{\rm dc1}$ is the minimum voltage level of dc bus, a is the overloading factor, V is the phase voltage, I is the phase current, and t is the time by which the dc bus voltage is to be recovered.

Considering the minimum voltage level of the dc bus, $V_{\rm dc1} =$ 690 V, $V_{\rm dc} = 700$ V, $V = 239.60$ V, $I = 27.82$ A, $t = 350$ μs, $a = 1.2$, the calculated value of $C_{\rm dc}$ is 2600 μF and is selected as 3000 μF.

C. AC Inductor

The selection of the ac inductance (L_f) of VSC depends on the current ripple $i_{\rm cr,p\text{-}p}$, switching frequency f_s, dc bus voltage ($V_{\rm dc}$), and L_f is given as [17]

$$L_f = \frac{\sqrt{3}mV_{\rm dc}}{12af_s i_{\rm cr(p\text{-}p)}} \tag{3}$$

where m is the modulation index and a is the overload factor. Considering, $i_{\rm cr,p\text{-}p} = 5\%$, $f_s = 10$ kHz, $m = 1$, $V_{\rm dc} = 700$ V, $a = 1.2$, the L_f value is calculated to be 2.44 mH. A round-off value of L_f of 2.5 mH is selected in this investigation.

D. Ripple Filter

A low-pass first-order filter tuned at half the switching frequency is used to filter the high-frequency noise from the voltage at the PCC. Considering a low impedance of 8.1 Ω for the harmonic voltage at a frequency of 5 kHz, the ripple filter capacitor is designed as $C_f = 5$ μF. A series resistance (R_f) of 5 Ω is included in series with the capacitor (C_f). The impedance is found to be 637 Ω at fundamental frequency, which is sufficiently large, and hence, the ripple filter draws negligible fundamental current.

E. Design of the T-connected Transformer

Fig. 3(a) shows the connection of two single-phase transformers in T-configuration for interfacing with a three-phase

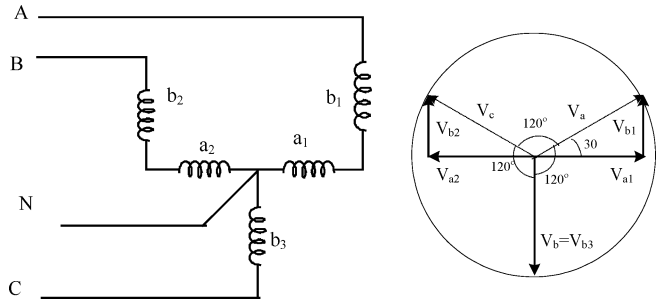

Fig. 3. (a) T-connected transformer and the three-leg VSC. (b) Phasor diagram.

four-wire system. The T-connected windings of the transformer not only provide a path for the zero-sequence fundamental current and harmonic currents but also offer a path for the neutral current when connected in shunt at point of common coupling (PCC). Under unbalanced load, the zero-sequence load-neutral current divides equally into three currents and takes a path through the T-connected windings of the transformer. The current rating of the windings is decided by the required neutral current compensation. The voltages across each winding are designed as shown shortly.

The phasor diagram shown in Fig. 3(b) gives the following relations to find the turn's ratio of windings. If V_{a1} and V_{b1} are the voltages across each winding and V_a is the resultant voltage, then

$$V_{a1} = K_1 V_a \tag{4}$$

$$V_{b1} = K_2 V_a \tag{5}$$

where K_1 and K_2 are the fractions of winding in the phases. Considering $|V_a| = |V_b| = V$ and $V_{a1} = V_a \cos 30^\circ$, $V_{b1} = V_a \sin 30^\circ$, then from (4) and (5), one gets, $K_1 = 0.866$ and $K_2 = 0.5$.

The line voltage is $V_{ca} = 415$ V

$$V_a = V_b = V_c = \frac{415}{\sqrt{3}} = 239.60 \text{ V} \tag{6}$$

$$V_{a1} = 207.49 \text{ V}, \qquad V_{b1} = 119.80 \text{ V}. \tag{7}$$

Hence, two single-phase transformers of rating 5 kVA, 240 V/120 V/120 V and 5 kVA, 208 V/208 V are selected.

III. Control of DSTATCOM

The control approaches available for the generation of reference source currents for the control of VSC of DSTATCOM for three-phase four-wire system are instantaneous reactive power theory (IRPT), synchronous reference frame theory (SRFT), unity power factor (UPF) based, instantaneous symmetrical components based, etc. [12], [13]. The SRFT is used in this investigation for the control of the DSTATCOM. A block diagram of the control scheme is shown in Fig. 4. The load currents (i_{La}, i_{Lb}, i_{Lc}), the PCC voltages (v_{Sa}, v_{Sb}, v_{Sc}), and dc bus voltage ($v_{\rm dc}$) of DSTATCOM are sensed as feedback signals. The load currents from the a–b–c frame are first converted to the

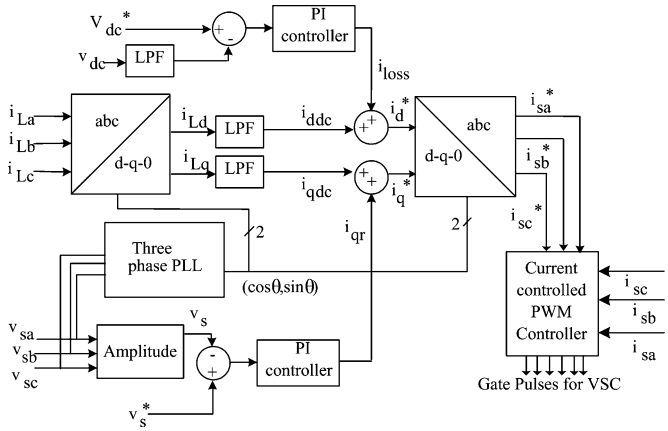

Fig. 4. Control algorithm for the three-leg-VSC-based DSTATCOM in a three-phase four-wire system.

α–β–o frame and then to the d–q–o frame using

$$\begin{bmatrix} i_{Lq} \\ i_{Ld} \\ i_{L0} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \sin\theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{8}$$

where $\cos\theta$ and $\sin\theta$ are obtained using a three-phase phase-locked loop (PLL). A PLL signal is obtained from terminal voltages for generation of fundamental unit vectors [18] for conversion of sensed currents to the d–q–o reference frame. The SRF controller extracts dc quantities by a low-pass filter, and hence, the non-dc quantities (harmonics) are separated from the reference signal. The d-axis and q-axis currents consist of fundamental and harmonic components as

$$i_{Ld} = i_{d\,\rm dc} + i_{d\,\rm ac} \tag{9}$$

$$i_{Lq} = i_{q\,\rm dc} + i_{q\,\rm ac}. \tag{10}$$

A. UPF Operation of DSTATCOM

The control strategy for reactive power compensation for UPF operation considers that the source must deliver the mean value of the direct-axis component of the load current along with the active power component current for maintaining the dc bus and meeting the losses ($i_{\rm loss}$) in DSTATCOM. The output of the proportional-integral (PI) controller at the dc bus voltage of DSTATCOM is considered as the current ($i_{\rm loss}$) for meeting its losses

$$i_{{\rm loss}(n)} = i_{{\rm loss}(n-1)} + K_{pd}(v_{de(n)} - v_{de(n-1)}) + K_{id} v_{de(n)} \tag{11}$$

where $v_{de(n)} = v^*_{\rm dc} - v_{{\rm dc}(n)}$ is the error between the reference ($v^*_{\rm dc}$) and sensed ($v_{\rm dc}$) dc voltages at the nth sampling instant. K_{pd} and K_{id} are the proportional and integral gains of the dc bus voltage PI controller.

The reference source current is therefore

$$i_d^* = i_{d\,\mathrm{dc}} + i_{\mathrm{loss}}. \tag{12}$$

The reference source current must be in phase with the voltage at the PCC but with no zero-sequence component. It is therefore obtained by the following reverse Park's transformation with i_d^* as in (12) and i_q^* and i_0^* as zero

$$\begin{bmatrix} i_a^* \\ i_b^* \\ i_c^* \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta & 1 \\ \cos\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta - \frac{2\pi}{3}\right) & 1 \\ \cos\left(\theta + \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) & 1 \end{bmatrix} \begin{bmatrix} i_d^* \\ i_q^* \\ i_0^* \end{bmatrix}. \tag{13}$$

B. Zero-Voltage Regulation (ZVR) Operation of DSTATCOM

The compensating strategy for ZVR operation considers that the source must deliver the same direct-axis component i_d^*, as mentioned in (12) along with the sum of quadrature-axis current ($i_{q\,\mathrm{dc}}$) and the component obtained from the PI controller (i_{qr}) used for regulating the voltage at PCC. The amplitude of ac terminal voltage (V_S) at the PCC is controlled to its reference voltage (V_S^*) using the PI controller. The output of PI controller is considered as the reactive component of current (i_{qr}) for zero-voltage regulation of ac voltage at PCC. The amplitude of ac voltage (V_S) at PCC is calculated from the ac voltages (v_{sa}, v_{sb}, v_{sc}) as

$$V_S = (2/3)^{1/2}(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)^{1/2}. \tag{14}$$

Then, a PI controller is used to regulate this voltage to a reference value as

$$i_{qr(n)} = i_{qr(n-1)} + K_{pq}(v_{te(n)} - v_{te(n-1)}) + K_{iq}v_{te(n)} \tag{15}$$

where $v_{te(n)} = V_S^* - V_{S(n)}$ denotes the error between reference (V_S^*) and actual ($V_{S(n)}$) terminal voltage amplitudes at the nth sampling instant. K_{pq} and K_{iq} are the proportional and integral gains of the dc bus voltage PI controller. The reference source quadrature-axis current is

$$i_q^* = i_{q\,\mathrm{dc}} + i_{qr}. \tag{16}$$

The reference source current is obtained by reverse Park's transformation using (13) with i_d^* as in (12) and i_q^* as in (16) and i_0^* as zero.

C. Computation of Controller Gains

The gains of the controllers are obtained using the Ziegler–Nichols step response technique [19]. A step input of amplitude (U) is applied and the output response of the dc bus voltage is obtained for the open-loop system. The maximum gradient (G) and the point at which the line of maximum gradient crosses the time axis (T) are computed. The gains of the controller are computed using the following equations:

$$K_p = \left|\frac{1.2U}{GT}\right| \tag{17}$$

$$K_i = \left|\frac{0.6U}{GT^2}\right|. \tag{18}$$

The gain values for both the PI controllers are computed and are given in the Appendix.

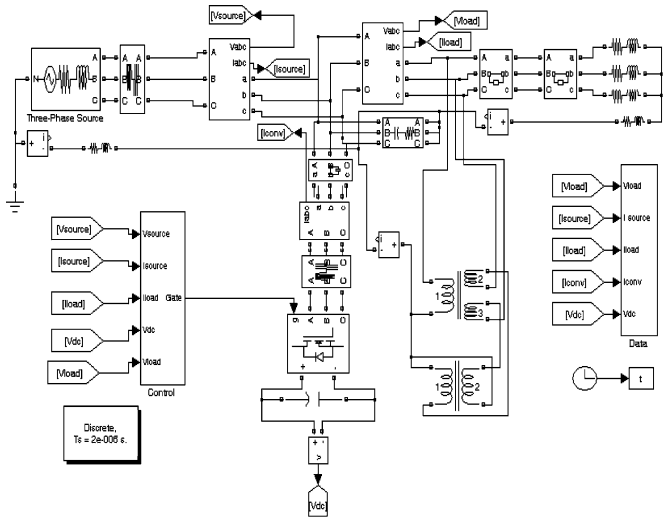

Fig. 5. MATLAB model of the T-connected transformer and the three-leg-VSC-based DSTATCOM-connected system.

D. Current-Controlled Pulsewidth Modulation (PWM) Generator

In a current controller, the sensed and reference source currents are compared and a proportional controller is used for amplifying current error in each phase before comparing with a triangular carrier signal to generate the gating signals for six IGBT switches of VSC of DSTATCOM.

IV. Modeling and Simulation

The three-leg VSC and the T-connected-transformer-based DSTATCOM connected to a three-phase four-wire system is modeled and simulated using the MATLAB with its Simulink and PSBs. The ripple filter is connected to the DSTATCOM for filtering the ripple in the PCC voltage. The system data are given in the Appendix. The MATLAB-based model of the three-phase four-wire DSTATCOM is shown in Fig. 5. The T-connected transformer in parallel to the load, the three-phase source, and the shunt-connected three-leg VSC are connected as shown in Fig. 5. The available model of linear transformers, which includes losses, is used for modeling the T-connected transformer.

The control algorithm for the DSTATCOM is also modeled in MATLAB. The reference source currents are derived from the sensed PCC voltages (v_{sa}, v_{sb}, v_{sc}), load currents (i_{La}, i_{Lb}, i_{Lc}), and the dc bus voltage of DSTATCOM (v_{dc}). A PWM current controller is used over the reference and sensed source currents to generate the gating signals for the IGBTs of the VSC of the DSTATCOM.

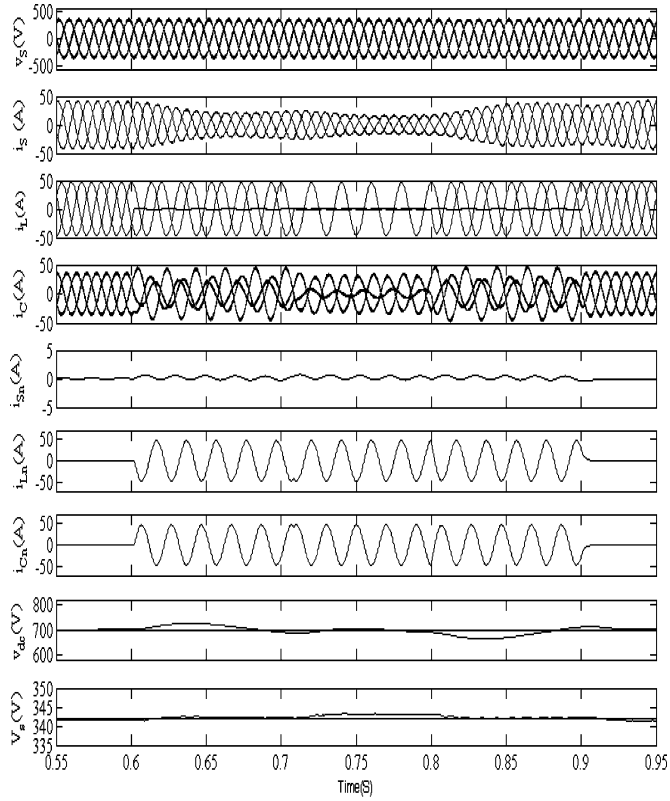

Fig. 6. Performance of a three-phase three-leg VSC and T-connected transformer-based DSTATCOM for neutral current compensation, load balancing, and voltage regulation.

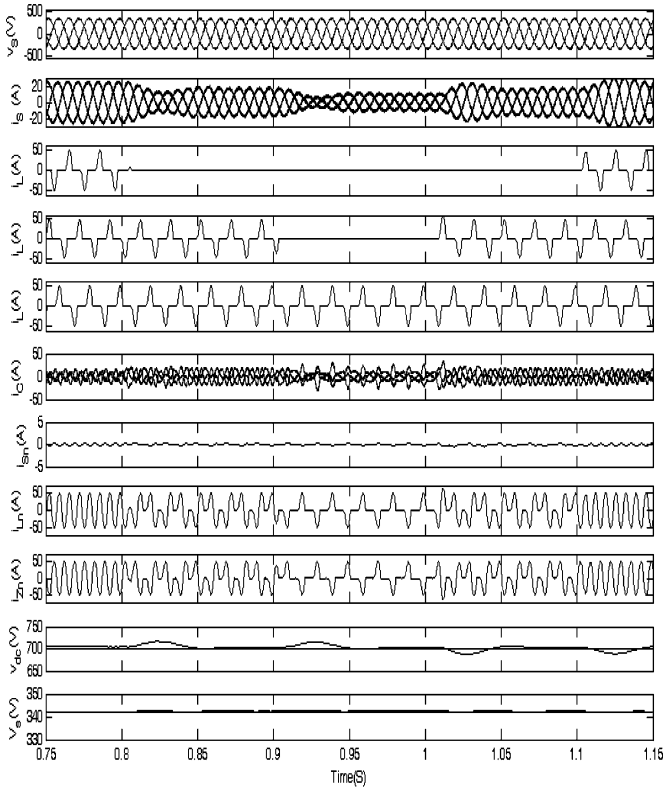

Fig. 7. Performance of a three-phase three-leg VSC and T-connected transformer-based DSTATCOM for neutral current compensation, load balancing, harmonic compensation, and voltage regulation.

V. Results and Discussion

The performance of the T-connected transformer and three-leg-VSC-based three-phase four-wire DSTATCOM is demonstrated for power factor correction and voltage regulation along with harmonic reduction, load balancing, and neutral current compensation. The developed model is analyzed under varying loads and the results are discussed shortly.

A. Performance of DSTATCOM With Linear Load for Neutral Current Compensation, Load Balancing, and ZVR Operation

The dynamic performance of the DSTATCOM under linear lagging power factor unbalanced load condition is shown in Fig. 6. At 0.6 s, the load is changed to two-phase load and to single-phase load at 0.7 s. These loads are applied again at 0.8 and 0.9 s, respectively. The PCC voltages (v_S), source currents (i_S), load currents (i_L), compensator currents (i_C), source-neutral current (i_{Sn}), load-neutral current (i_{Ln}), compensator-neutral current (i_{Cn}), dc bus voltage ($v_{\rm dc}$), and amplitude of voltage (V_S) at PCC are also depicted in Fig. 6. The source-neutral current is observed as nearly zero, and this verifies the proper compensation. It is also observed that the dc bus voltage of DSTATCOM is able to maintain close to the reference value under all disturbances. The amplitude of PCC voltage is maintained at the reference value under various load disturbances, which shows the ZVR mode of operation of DSTATCOM.

B. Performance of DSTATCOM With Nonlinear Load for Harmonic Compensation, Load Balancing, and ZVR Operation

The dynamic performance of the DSTATCOM with nonlinear and unbalanced load is given in Fig. 7. It is observed that the harmonic current is compensated and the source currents are balanced and sinusoidal. At 0.8 s, the load is changed to two-phase load and to single-phase load at 0.9 s. The loads are applied again at 1.0 and 1.1 s, respectively. The source currents are still balanced and sinusoidal even when the load current in a phase is zero. The dc bus voltage of DSTATCOM is maintained at nearly its reference value under all load disturbances.

C. Performance of DSTATCOM With Linear Load for Neutral Current Compensation, Load Balancing, and UPF Operation

The dynamic performance of the DSTATCOM during linear-lagging power-factor-unbalanced load condition is depicted in Fig. 8. At 0.6 s, the load is changed to two-phase load and to single-phase load at 0.7 s. The loads are applied again at 0.8 and 0.9 s, respectively. The PCC voltages (v_S), source currents (i_S), load currents (i_L), compensator currents (i_C), source-neutral current (i_{Sn}), load-neutral current (i_{Ln}), compensator-neutral current (i_{Cn}), dc bus voltage ($v_{\rm dc}$), and amplitude of voltage (V_S) at PCC are also depicted in Fig. 8. The reactive power is compensated for power factor correction, and the source currents are balanced and sinusoidal. The source-neutral current is nearly

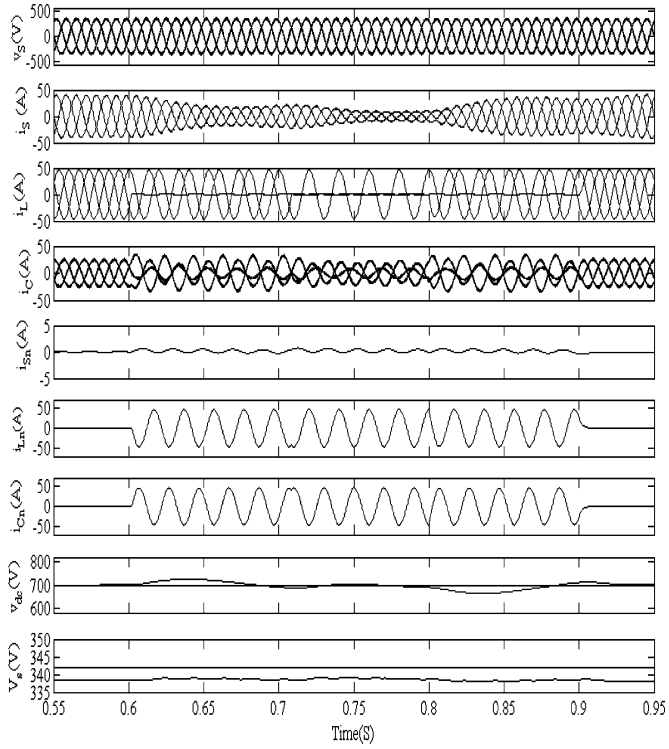

Fig. 8. Performance of a three-phase three-leg VSC and T-connected transformer-based DSTATCOM for neutral current compensation, load balancing, and power factor correction.

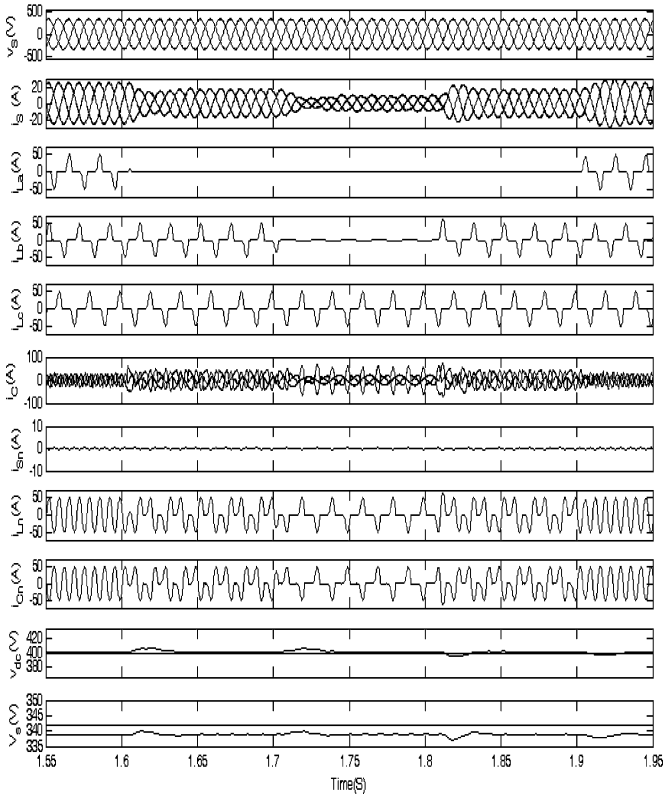

Fig. 9. Performance of a three-phase three-leg VSC and T-connected transformer-based DSTATCOM for neutral current compensation, load balancing, harmonic compensation, and power factor correction.

zero and it verifies the proper compensation. It is also observed that the dc bus voltage of DSTATCOM is maintained at the reference value under all load disturbances.

D. Performance of DSTATCOM With Nonlinear Load for Harmonic Compensation, Load Balancing, and UPF Operation

The dynamic performance of the DSTATCOM during nonlinear unbalanced load condition is shown in Fig. 9. The source currents are observed as balanced and sinusoidal under all these conditions. At 1.6 s, the load is changed to two-phase load and again to single-phase load at 1.7 s. The loads are applied again at 1.8 and 1.9 s, respectively. The PCC voltages (v_S), source currents (i_S), load currents (i_{La}, i_{Lb}, i_{Lc}), compensator currents (i_C), source-neutral current (i_{Sn}), compensator-neutral current (i_{Cn}), load-neutral current (i_{Ln}), dc bus voltage ($v_{\rm dc}$), and amplitude of voltage (V_S) at PCC are also depicted in Fig. 9. The dc bus voltage of DSTATCOM is maintained at the reference value under all load disturbances through proper control. The waveform of the load current, source current, and PCC voltage in one phase along with their harmonic spectra are demonstrated in Figs. 10–12, respectively. The total harmonic distortion of the source current is 1.72%, whereas that of the load current is 63.50%, and this shows the satisfactory performance of DSTATCOM for harmonic compensation as stipulated by the IEEE-519 standard.

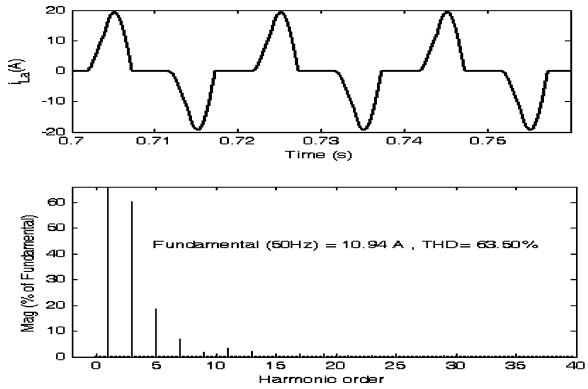

Fig. 10. Load current and the harmonic spectrum.

E. Experimental Demonstration of the Performance of T-Connected Transformer

The proposed topology of DSTATCOM consists of combined operation of three-leg VSC and a T-connected transformer. As the performance of a three-leg VSC and a zig-zag transformer is studied in [9], the T-connected transformer is analyzed for the compensation of neutral current. A prototype of the T-connected transformer is developed in the laboratory and the neutral current compensation technique is tested for linear and nonlinear loads. The T-connected transformer is tested for neutral current compensation under unbalanced linear loads and balanced/unbalanced nonlinear loads. When the load is

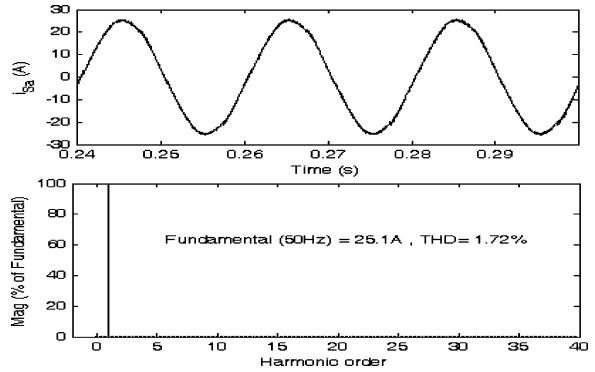

Fig. 11. Source current and the harmonic spectrum.

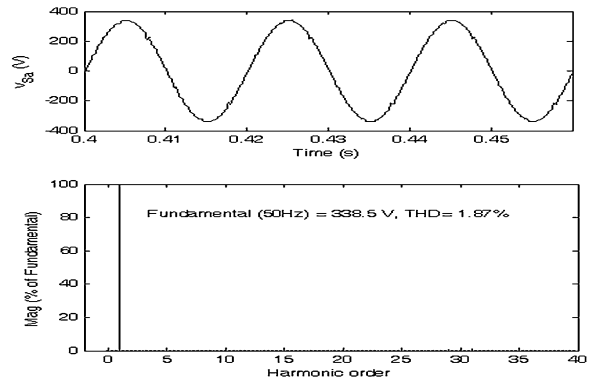

Fig. 12. Voltage at PCC with compensator.

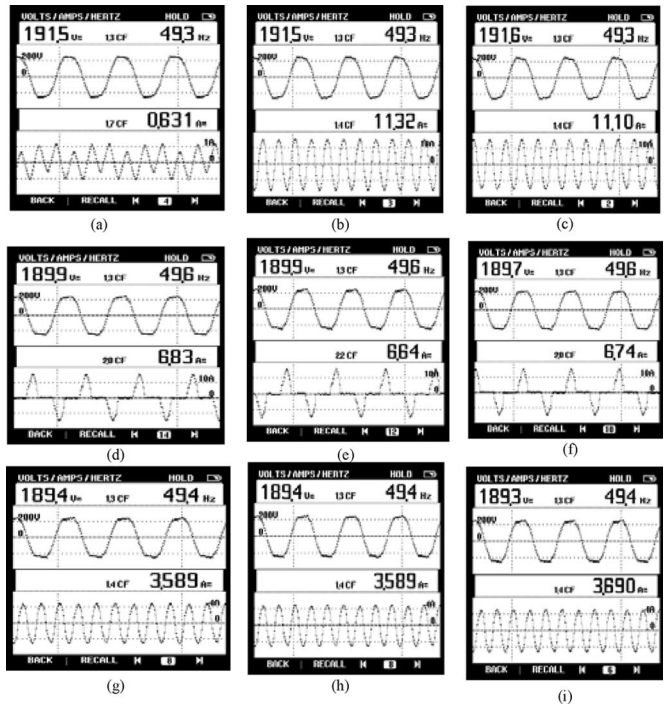

Fig. 13. Neutral current compensation using T-connected transformer. (a) Supply-neutral current. (b) Load-neutral current. (c) Transformer-neutral current. (d) Load current in phase "a." (e), Load current in phase "b." (f) Load current in phase "c." (g) Transformer current in phase "a." (h) Transformer current in phase "b." (i) Transformer current in phase "c."

nonlinear and balanced, the load-neutral current is observed to be mainly triplen harmonics current, and this is compensated using the T-connected transformer. The source-neutral current, load-neutral current, and the transformer-neutral current are shown in Fig. 13(a)–(c), respectively. The source-neutral current is 0.63 A when the load current is 11.32 A. The load-neutral current is circulated in the T-connected transformer, as evident from the 11.10 A current. The load-neutral currents are shown in Fig. 13(d)–(f). They are nearly equal and are high in harmonic currents. The T-connected transformer currents are shown in Fig. 13(g)–(i). The transformer currents are almost equal in all phases and are one-third of the transformer-neutral current.

VI. Comparison With Other Techniques

A three-leg single-phase-VSC-based DSTATCOM [3] requires a total of 12 semiconductor devices, and hence, is not attractive, and the three-leg VSC with split capacitors [3] has the disadvantage of difficulty in maintaining equal dc voltage at two series-connected capacitors. The four-leg-VSC-based DSTATCOM [3] is considered as superior considering the number of switches, complexity, cost, etc. A three-leg VSC with zig-zag transformer [9] is reported recently and has shown improved performance. The three-leg VSC with zig-zag transformer has the advantage of using a passive device for neutral current compensation, reduced number of switches, use of readily available three-leg VSC, etc.

TABLE I
Comparison of Rating of Transformer Connections for Neutral Current Compensation

Transfo-rmer	winding Voltage (V)	winding Current (A)	kVA	Numbe r of Transfo rmers	Total kVA
Zig-zag	140/140	10	1.4	3 Nos	4.2
Star/ Delta	240/240	10	2.4	3 Nos	7.2
T-connected	240/120/120 208/208	10	2.4 2.08	1 Nos 1Nos	4.48

The proposed three-phase four-wire DSTATCOM is based on a three-leg VSC and a T-connected transformer. The T-connected transformer requires two single-phase transformers, whereas the zig-zag transformer reported in [9] has three single-phase transformers with a turn's ratio of 1:1. The total kilovolt.amperes rating of the transformers required for a given compensation is nearly equal in both cases. A star/delta transformer is also reported [20] for neutral current compensation and the kVA rating required is higher compared to T-connected transformer. Table I shows the rating comparison of the three transformer techniques for a given neutral current of 10 A. It is observed that the kVA rating of the T-connected transformer is

much less compared to a star/delta transformer. Similarly, comparison with the four-leg converter shows that the number of switches are reduced in the proposed configuration, thus reducing the complexity and cost of the system. But the disadvantage of the proposed topology is that it requires a special transformer, and also the proper compensation is affected by the impedance of the transformer similarly to that demonstrated for a zig-zag transformer [9].

VII. Conclusion

The performance of a new topology of three-phase four-wire DSTATCOM consisting of three-leg VSC with a T-connected transformer has been demonstrated for neutral current compensation along with reactive power compensation, harmonic elimination, and load balancing. The T-connected transformer has mitigated the source-neutral current. The voltage regulation and power factor correction modes of operation of the DSTATCOM have been observed and are as expected. The dc bus voltage of the DSTATCOM has been regulated to the reference dc bus voltage under all varying loads. Two single-phase transformers are used for the T-configuration of the transformer to interface with a three-phase four-wire system. The total kilovolt·amperes rating of the T-connected transformer is lower than a star/delta transformer for a given neutral current compensation. The experimental results on a prototype have verified that the T-connected transformer has been effective in compensating the zero sequence fundamental and harmonics currents.

Appendix

Line impedance: $R_s = 0.01\ \Omega$, $L_s = 2$ mH
Loads: 1) linear: 20 kV·A, 0.80 pF lag
2) Nonlinear: Three single-phase bridge rectifiers with $R = 25\ \Omega$ and $C = 470\ \mu$F
Ripple filter: $R_f = 5\ \Omega$, $C_f = 5\ \mu$F
DC bus voltage of DSTATCOM: 700 V
DC bus capacitance of DSTATCOM: 3000 μF
AC inductor: 2.5 mH
DC voltage PI controller: $K_{pd} = 0.19$, $K_{id} = 6.25$
PCC voltage PI controller: $K_{pq} = 0.9$, $K_{iq} = 7.5$
AC line voltage: 415 V, 50 Hz
PWM switching frequency: 10 kHz
T-connected transformer: Two single-phase transformers of rating 5 kVA, 240 V/120 V/120 V and 5 kVA, 208 V/208 V.

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