A Grid-Interfacing Power Quality Compensator for Three-Phase Three-Wire Microgrid Applications

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***Abstract*—This paper proposes a grid-interfacing power quality compensator for three-phase three-wire microgrid applications with consideration of both the power quality of the microgrid and the quality of currents flowing between the microgrid and utility system. It is proposed that two inverters connected in shunt and series are used for each distributed generation (DG) system in the microgrid. In each inverter, both positive- and negative-sequence components are controlled to compensate for the effects caused by the unbalanced utility grid voltages. Specifically, the shunt inverter is controlled to ensure balanced voltages within the microgrid and to regulate power dispatches among parallel-connected DG systems, while the series inverter balances the line currents by injecting appropriate voltage components. A current-limiting algorithm is also proposed and integrated within the inverter control schemes to protect the microgrid from large fault currents during utility voltage sags. The proposed compensator has been tested in simulations and experimentally using a laboratory hardware prototype.**

***Index Terms*—Fault current limitation, flux-charge-model control, microgrid, positive- and negative-sequence, power quality compensator.**

I. Introduction

MICROGRIDS are systems with clusters of micro-generators, which are installed for distributed power generation [1]. These micro-generators are usually connected to the utility grid using voltage source inverter based interfaces, where a case of concern related to this interfacing is the impact of unbalanced grid voltages (usually caused by unbalanced system faults or connected loads) on the overall system performance. If the unbalance in voltages is serious, the solid-state circuit breaker, connected between the microgrid and utility grid as in Fig. 1, will open to isolate the microgrid. But when the voltage unbalance is not so serious, the circuit breaker may remain closed, resulting in sustained unbalanced voltages at the point of common coupling (PCC). Such a voltage unbalance can cause an increase in losses in motor loads (and hence motor overheating) and abnormal operation of sensitive equipment in the microgrid, etc. [2].

An obvious solution to the above-mentioned problem is to balance the sensitive load voltages in the microgrid using some voltage regulation techniques. However large unbalanced currents can flow between the unbalanced utility grid and microgrid due to the very low line impedance interfacing both grids, if only the microgrid voltages are regulated [3]. This flow of large unbalanced currents can over-stress semiconductor devices within the interfacing inverters and system components such as overhead lines and feeder cables. This problem is particularly of concern during utility voltage sags, when large difference between the utility and microgrid voltages causes severe fault currents to flow along the low impedance distribution feeder for a few fundamental cycles.

Therefore, to control both the sensitive load voltages in the microgrid and the line currents flowing between the microgrid and utility system, a grid-interfacing power quality compensator using two inverters (inverters A and B) is proposed for each DG system, as illustrated in Fig. 1. The main functions of shunt inverter A are to maintain a balanced set of sensitive load voltages in the microgrid under all grid and load operating conditions, generate and dispatch power, share the power demand with other parallel-connected DG systems when the microgrid operates in islanding mode, and to synchronize the microgrid with the utility system at the instant of connection. The main functions of series inverter B are to inject appropriate voltage components along the distribution feeder to balance the line currents flowing between the microgrid and unbalanced utility grid, and to limit the flow of large fault currents during utility voltage sags. These control objectives of the proposed compensator are different from those of other reported power conditioners [e.g., unified power quality conditioners (UPQCs)], whose series inverter is controlled to balance the load terminal voltages by appropriate series voltage injection, and shunt inverter is controlled to inject harmonic compensating currents to shape the utility currents drawn as balanced sinusoids. Therefore, for the proposed compensator, the development of an appropriate control algorithm is challenging since existing control algorithms are not directly applicable. This control development is presented in the following sections of the paper.

II. Control Of Power Quality Compensator

A. Control of Shunt Inverter A

As shown in Fig. 2, the control scheme of shunt inverter A contains internal voltage/current regulation loops and external power control loops. The detailed design of the power control loops has already been presented by the authors in [4] and therefore is not duplicated in this paper. Here attention is focused on the design of shunt inverter A internal voltage/current control loops, after an introductory description of the power control loops to give an overview of the functionalities of shunt inverter A.

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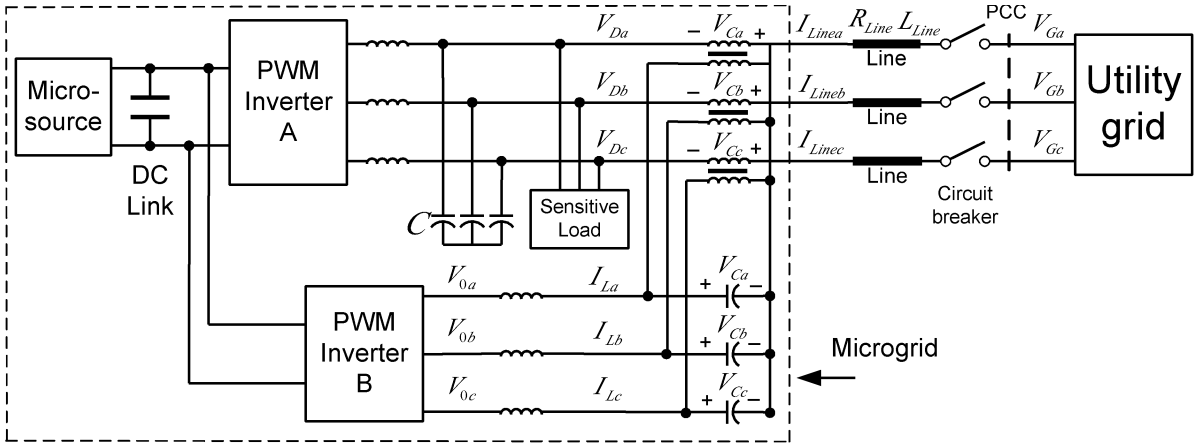


Fig. 1. Proposed microgrid configuration.

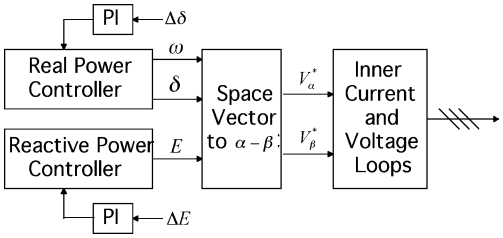


Fig. 2. Overall control structure of shunt inverter A.

In brief, the power loops are designed to control real and reactive power flow, and facilitate power sharing between the paralleled DG systems when a utility fault occurs and the microgrid operates in islanding mode. The power loops achieve this appropriate sharing of power by producing the desired command frequency ω, phase δ and positive-sequence voltage magnitude E, which are subsequently transformed into the stationary-frame references of V_α^*, V_β^* to be used in the internal voltage/current regulation loops. Ideally, the power loops should perform these reference calculations independently with no physical communication link between the DG systems, and can conveniently be implemented by introducing artificial "real power versus supply frequency" and "reactive power versus voltage magnitude" droop characteristics to the power loops. Furthermore, since the outputs of the power loops contain only positive-sequence components, the calculation of these outputs is independent of the series inverter outputs, which consist of only negative-sequence components when the power loops are functioning. The detailed control and functions of the series inverter are presented in the next subsection and Section III.

Besides power control, the external power loops also govern the synchronization of microgrid and utility to ensure smooth and safe reconnection of the two grids when the fault is cleared and the system returns to grid-connected mode of operation. Synchronization can be achieved by aligning the voltage phasors at the microgrid and utility ends of the circuit breaker shown in Fig. 1, and can conveniently be implemented by adding two separate synchronization PI regulators to the external real and reactive power control loops. As shown in Fig. 2, inputs to these synchronization regulators are the magnitude ΔE and phase $\Delta\delta$ errors of the two voltage phasors at both ends of the circuit breaker. Their outputs are then fed to the real and reactive power loops to make the voltage phasor at the microgrid end tracks the phasor at the utility end closely both in magnitude and frequency (PI regulators forcing $\Delta E \to 0$ and $\Delta\delta \to 0$).

Fig. 3 shows the voltage control scheme of shunt inverter A, which contains an inner filter inductor current control loop and an outer load voltage control loop. For the outer voltage loop, alternative second-order stationary-frame controllers with zero tracking errors and a higher computational efficiency (details presented later in the section) are chosen for this work. Theoretically, these second-order controllers can be derived by transforming PI controllers from the synchronous to the stationary frame. A systematic method for presenting the voltage control loop is therefore to first present the theoretical analysis in the positive- and negative-sequence reference frames rotating in the opposite directions (see control block diagram enclosed within dotted box in Fig. 3), and subsequently convert the developed synchronous voltage controllers to the stationary frame.

As illustrated in Fig. 3, the three-phase line-to-line load voltages are first transformed from the stationary a-b-c frame to the stationary $\alpha-\beta\{V_\alpha, V_\beta\}$ by using

$$A = \begin{bmatrix} \sqrt{\frac{2}{3}} & -\sqrt{\frac{1}{6}} & -\sqrt{\frac{1}{6}} \\ 0 & \frac{\sqrt{2}}{2} & -\frac{\sqrt{2}}{2} \end{bmatrix} * \begin{bmatrix} \frac{1}{3} & 0 & -\frac{1}{3} \\ -\frac{1}{3} & \frac{1}{3} & 0 \\ 0 & -\frac{1}{3} & \frac{1}{3} \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{1}{6}} & 0 & -\sqrt{\frac{1}{6}} \\ \frac{-\sqrt{2}}{6} & \frac{\sqrt{2}}{3} & \frac{-\sqrt{2}}{6} \end{bmatrix}$$

(where the first matrix is for transforming the phase quantities from a-b-c frame to $\alpha-\beta$ frame and the second matrix is for transforming the measured line voltages to phase voltages) before subtracted from their reference values $\{V_\alpha^*, V_\beta^*\}$ to give the voltage errors $\{e_\alpha, e_\beta\}$. An obvious way for ensuring zero tracking errors is to first convert the stationary $\alpha-\beta$ voltage errors to their positive- and negative-sequence components $\{e_d^+, e_q^+, e_d^-, e_q^-\}$ by using the d–q synchronous transformation matrices $T_1 = \begin{bmatrix} \mathrm{Cos}(\omega t) & \mathrm{Sin}(\omega t) \\ -\mathrm{Sin}(\omega t) & \mathrm{Cos}(\omega t) \end{bmatrix}$ and $T_2 = \begin{bmatrix} \mathrm{Cos}(\omega t) & -\mathrm{Sin}(\omega t) \\ -\mathrm{Sin}(\omega t) & -\mathrm{Cos}(\omega t) \end{bmatrix}$ (T_1 and T_2 is selected such that in

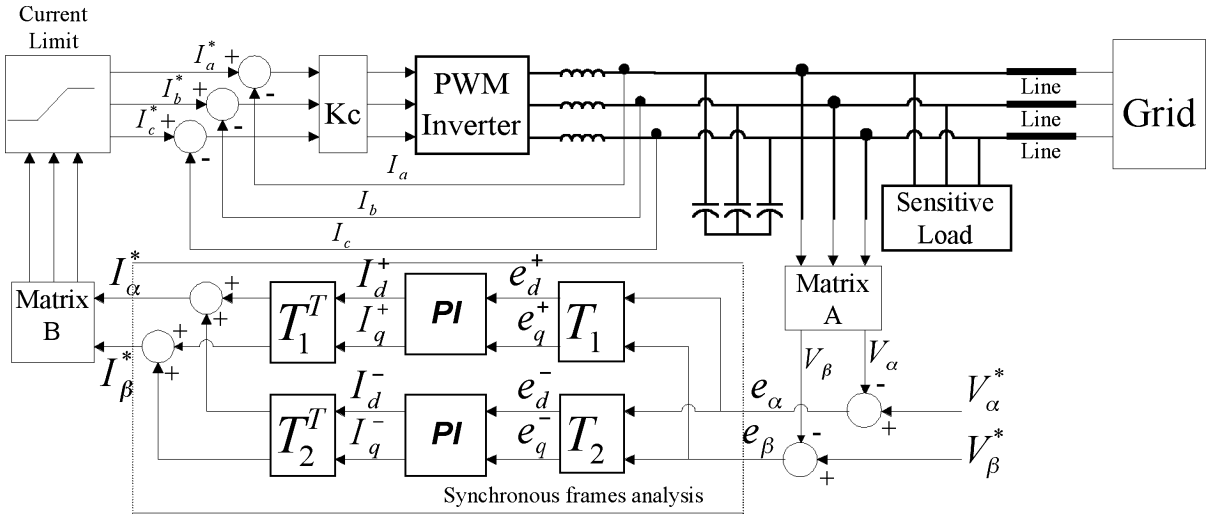


Fig. 3. Voltage control scheme of shunt inverter A.

both positive- and negative-sequence rotating frames, q axis is leading the d axis by 90°). These synchronous frames errors are then passed through two PI controllers placed along the control paths for eliminating the tracking errors.

While for easier physical implementation, a more practical form of the positive- and negative-sequence PI controllers can be derived by transforming the PI controllers to the stationary α–β frame [5]. Mathematically, these derived α–β frame controllers can be expressed as (assuming $k_p^+ = k_p^- = k_p$ and $k_i^+ = k_i^- = k_i$)

$$dY_{\alpha\beta}/dt = 2k_i e_{\alpha\beta} + Z_{\alpha\beta} \quad (1)$$

$$dZ_{\alpha\beta}/dt = -\omega^2 Y_{\alpha\beta} \quad (2)$$

$$I^*_{\alpha\beta} = Y_{\alpha\beta} + 2k_p e_{\alpha\beta} \quad (3)$$

$$H_{\alpha\beta} = [H_\alpha \quad H_\beta]^T; \quad H = e, Y, Z \text{ or } I^*$$

where $\{Y_{\alpha\beta}, Z_{\alpha\beta}\}, e_{\alpha\beta}$ and $I^*_{\alpha\beta}$ represent the state variables, voltage error inputs, and reference current outputs of the α–β frame controllers, respectively. Analyzing (1)(2)–(3), it is obvious that there is no cross coupling term in the α–β frame, and the equations can be expressed in the s-domain as (ω is the grid fundamental angular frequency) [6]

$$\begin{bmatrix} 2k_p + \frac{2k_i s}{s^2+\omega^2} & 0 \\ 0 & 2k_p + \frac{2k_i s}{s^2+\omega^2} \end{bmatrix}. \quad (4)$$

In this paper, (4) is used for implementing the voltage controllers as it allows processing of the α–β variables directly without any intermediate α–$\beta \leftrightarrow d$–q variable transformations [6], [7]. This method is not only computationally more efficient, but the steady-state voltage errors are also forced (both positive- and negative-sequence components) to zero by having infinite gains at frequencies $\pm\omega$.

The outputs of the voltage controllers are the sums of the positive- and negative-sequence reference inductor currents, expressed in the stationary frame as $\{I^*_\alpha, I^*_\beta\}$. These demanded reference current signals are transformed to the stationary a-b-c frame using matrix $B = \begin{bmatrix} \sqrt{\frac{2}{3}} & 0 \\ -\sqrt{\frac{1}{6}} & \frac{\sqrt{2}}{2} \\ -\sqrt{\frac{1}{6}} & -\frac{\sqrt{2}}{2} \end{bmatrix}$, and fed into the inner current control loop with peak current limiting capability. This inner current loop is implemented using only proportional controllers K_c with the three-phase inductor currents chosen as feedback variables, since it does not influence the tracking accuracy of the outer voltage loop. With the chosen voltage and current controllers, and representing the inner current loop as a constant gain block (due to its dynamically fast response), the closed-loop "output voltage to reference" transfer function of shunt inverter A is derived as (5) (note that (5) is valid for both grid-connected and islanding modes, and a second "output voltage to load current" transfer function can be derived, but is not explicitly shown here since the system can easily be made load-insensitive by using relatively large controller gains). Its corresponding bode plot is shown in Fig. 4 with k_p and k_i chosen

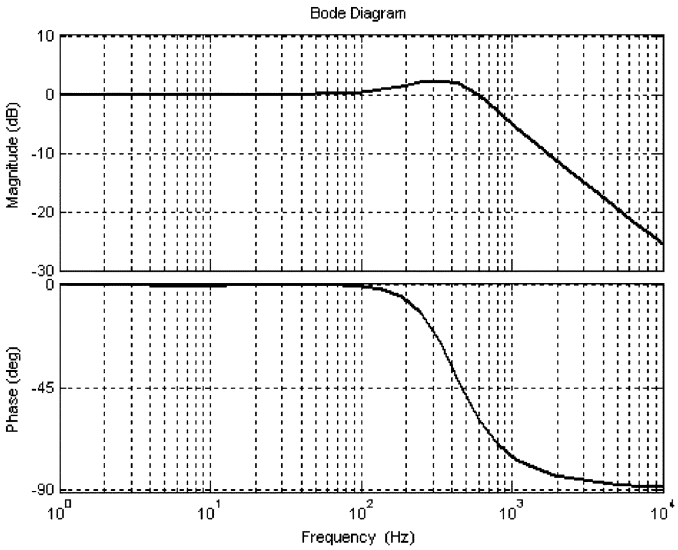


Fig. 4. Bode plot of closed-voltage-loop of shunt inverter A.

TABLE I
SYSTEM PARAMETERS

Parameter	Value
Nominal line-to-line grid voltage	120V
Frequency	50Hz
DC supply voltage	250V
Switching frequency for both inverters	10kHz
Series inverter filter capacitance	10μF
Series inverter filter inductance	3.9mH
Series transformer turns ratio	1:1
Shunt inverter filter capacitance	30μF
Shunt inverter filter inductance	5mH
Line resistance R_{Line}	3Ω
Line inductance L_{Line}	10mH
Grid dispatch power	300W, 160Var
Sensitive load in the microgrid	120W, 90Var

as 0.05 and 100, respectively (other system parameters are listed in Table I). This figure shows the controller good performance at the fundamental frequency and its immunity to high frequency distortion

$$V_D = \frac{2k_p s^2 + 2k_i s + 2\omega^2 k_p}{Cs^3 + 2k_p s^2 + (\omega^2 C + 2k_i)s + 2\omega^2 k_p} V^*. \quad (5)$$

B. Control of Series Inverter B

The circuit connection of series inverter B is shown in Fig. 1. For the proposed microgrid application, this series inverter is controlled to maintain a balanced set of line currents ($I_{\mathrm{Line}a}$, $I_{\mathrm{Line}b}$, and $I_{\mathrm{Line}c}$) along the distribution feeder by suppressing negative-sequence current flow through the injection of appropriate negative-sequence voltages (V_{Ca}, V_{Cb}, and V_{Cc}). Controlled in this way, series inverter B is expected to supply zero real and reactive power to the grid system as it injects only negative-sequence voltages along the feeder, which now conducts only positive-sequence currents. Obviously, this method of control is different from that used in a series dynamic voltage restorer (DVR) whose main functionality is to improve the downstream load voltage quality by generating suitable series voltages to compensate for the upstream utility voltage dips. It is also commented here that the series inverter is not designed for controlling the positive-sequence currents in this mode of operation, since these are already (directly) regulated by shunt inverter A.

Fig. 5 shows the control scheme for series inverter B, where an inner voltage loop is shown embedded within an outer current loop. The outer current loop (also referred to as the reference voltage generator) functions to generate reference voltages for the inner voltage loop using the negative-sequence line currents as inputs. As seen, the measured line currents are first transformed to the negative synchronous reference frame and then controlled to follow zero reference values. The outputs of this outer reference voltage generator, consisting only of negative-sequence components, are then transformed back to the α–β frame and fed into the inner voltage control loop. As this method of control to balance the line currents using a series inverter has not been recorded in the literature, its design will be covered in detail, as follows.

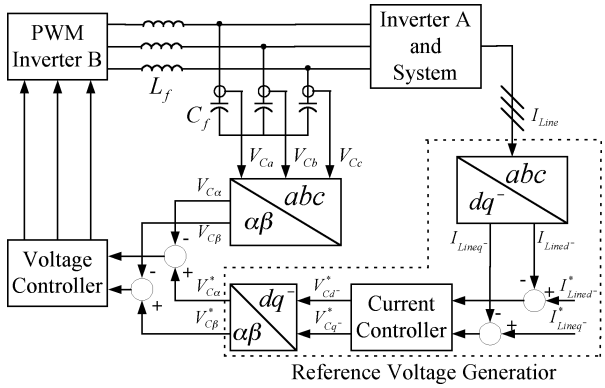


Fig. 5. Control scheme of series inverter B.

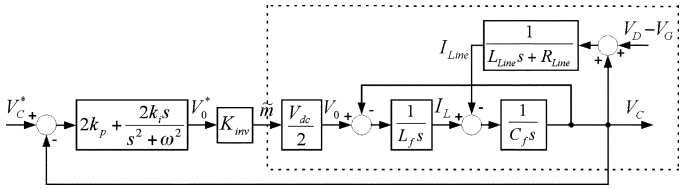


Fig. 6. Block diagram of closed-voltage-loop of series inverter B (Kinv = 2/Vdc).

As a common practice, the design of the proposed control algorithm for the series inverter begins with the voltage loop in the a–b frame. If open-loop voltage control is to be applied with pure negative-sequence reference voltages, the voltages generated at the series transformers will have both positive- and negative-sequence components. This is because although inverter B (unfiltered) output contains pure negative-sequence voltages, the positive-sequence line currents induce positive-sequence voltages across the filter inductors, which also appear across the series transformers. Therefore, to produce the desired pure negative-sequence voltages across the series injection transformers to balance the line currents, a closed-loop voltage control scheme is used, as shown in Fig. 6 where the voltage controllers used have the same form as that given in (4). Initial comparison between the controls of shunt inverter A and series inverter B might suggest that a filter inductor current loop can be embedded within the inner voltage loop of inverter B to improve its dynamic response. Further observation however reveals that the dynamics of inverter B is limited solely by the relatively slower outer reference voltage generation loop. Therefore, filter inductor current feedback is considered unnecessary and only a single voltage loop is used for this application.

For analysis, the closed-loop transfer function of Fig. 6 is derived and given in (6), shown at the bottom of the next page. Also shown are the Routh stability criteria of (7) and (8), which must be met for the inner voltage loop, to ensure stability. To confirm the robustness of inverter B control scheme, a typical distribution system where the line reactance is either the same or smaller than the line resistance [8], is considered. Here the series transformer leakage impedance is lumped together with the line impedance for simplicity. Even with an onerous condition of $X_{\mathrm{Line}} = (2\pi f)L_{\mathrm{Line}} = 2R_{\mathrm{Line}}$ for this distribution system, the stability condition (7) becomes $L_f - 2k_i R_{\mathrm{Line}}/\pi^2 f^2 > 0$, which can easily be met. Consequently, (8) can also be met since

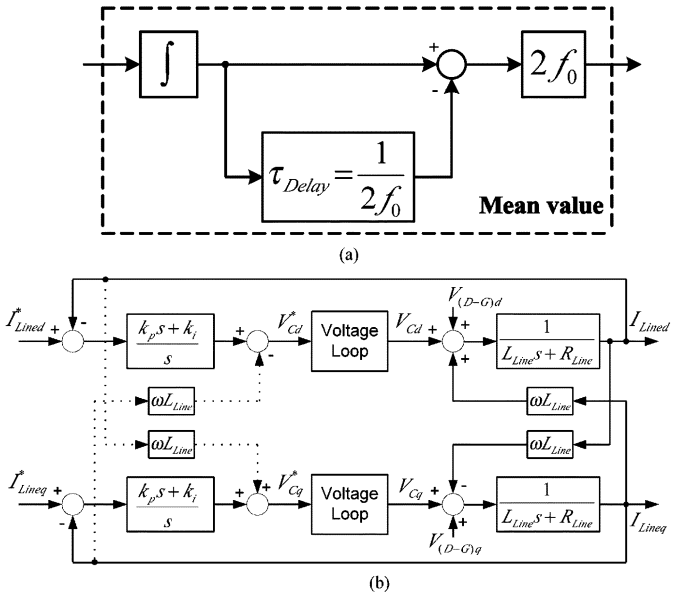


Fig. 7. Control of series inverter B in negative synchronous frame: (a) filtering of positive-sequence currents and (b) closed-current-loop.

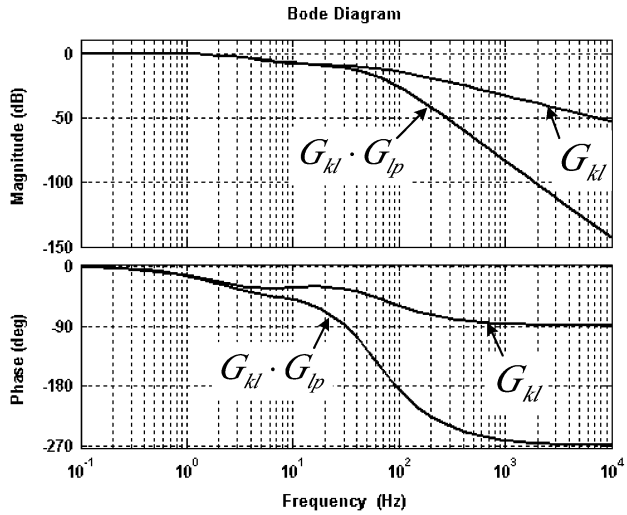


Fig. 8. Bode plots of $G_{\rm kl}$ and $G_{\rm kl}\cdot G{\rm lp}$.

the α term in (8) is now minimized by having a relatively larger denominator than numerator (the numerator is usually small due to the presence of a μF capacitive term C_f) as shown in (6)–(8) at the bottom of the page.

Once the design of the inner voltage loop is completed, the next step is to design the reference voltage generator in the negative synchronous frame. In the negative synchronous frame, negative-sequence line currents are transformed to dc signals, whereas positive-sequence currents are transformed to ac signals at twice the fundamental frequency. These ac signals should be filtered out to enhance the robustness of the control loop. In this paper, filtering is performed by averaging the currents over half a fundamental cycle in the negative synchronous frame, as shown in Fig. 7(a). Using Matlab control system toolbox to compute the second order Pade approximation of the transport delay block with $f_0 = 50$ Hz, the transfer function of the mean value calculation block can be expressed as

$$G_{\rm lp}=\frac{1-e^{-s/2f_0}}{s}2f_0=\frac{120000}{s^2+600s+30000}. \tag{9}$$

By representing the inner voltage loop as a unity gain (this is reasonable since the outer reference voltage generation loop is relatively slow), the series inverter connected system can be represented in the negative synchronous frame as in Fig. 7(b), where the coupling effects of the system are taken into account and measures have been taken to achieve decoupling (indicated by dotted lines in the figure). Analyzing this figure, the closed-current-loop transfer function for the d- and q-axes is derived as

$$G_{\rm kl}=\frac{k_p s+k_i}{L_{\rm Line}s^2+(R_{\rm Line}+k_p)s+k_i}. \tag{10}$$

Using (10) and choosing k_p as 1.5 and k_i as 80 for this work, the gain margin, phase margin and settling time of the outer voltage generation loop are set to infinity, 114^0 and 0.2 s, respectively. With further consideration of the dynamics of the mean value calculation filter, bode plots of $G_{\rm kl}$ and $G_{\rm kl}\cdot G_{\rm lp}$ are drawn in Fig. 8, where the bandwidths of $G_{\rm kl}$ and $G_{\rm kl}\cdot G_{\rm lp}$ remain close to each other due to the large difference of bandwidths between $G_{\rm kl}$ (3.4 Hz) and $G_{\rm lp}$ (43 Hz). This in turn ensures a stable and robust controller performance.

Another concern for the negative synchronous frame control is the requirement of angular frequency ω for the frame transformation. Normally, ω is obtained by a phase locked loop (PLL) algorithm, which accurately tracks the system frequency. While

$$G_{\rm Vcl}=\frac{k_pL_{\rm Line}s^3+(2k_pR_{\rm Line}+2k_iL_{\rm Line})s^2+(2k_p\omega^2L_{\rm Line}+2k_iR_{\rm Line})s+2k_p\omega^2R_{\rm Line}}{L_fC_fL_{\rm Line}s^5+L_fC_fR_{\rm Line}s^4+(L_f+L_{\rm Line}+2k_pL_{\rm Line}+L_fC_fL_{\rm Line}\omega^2)s^3+(2k_pR_{\rm Line}+2k_iL_{\rm Line}} \\ +R_{\rm Line}+L_fC_fR_{\rm Line}\omega^2)s^2+[(2k_p+1)\omega^2L_{\rm Line}+\omega^2L_f+2k_iR_{\rm Line}]s+(2k_p+1)\omega^2R_{\rm Line} \tag{6}$$

$$L_f-\frac{2k_iL_{\rm Line}^2}{R_{\rm Line}}>0 \tag{7}$$

$$2k_pR_{\rm Line}+2k_iL_{\rm Line}+R_{\rm Line}+L_fC_fR_{\rm Line}\omega^2-\frac{\overbrace{2k_iL_fC_fR_{\rm Line}^2+L_f^2C_fR_{\rm Line}\omega^2}^{\alpha}}{L_f-\frac{2k_iL_{\rm Line}^2}{R_{\rm Line}}}>0 \tag{8}$$

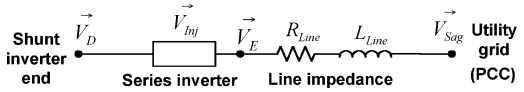


Fig. 9. Distribution feeder with specific voltages indicated.

for the microgrid, the tracking of frequency does not require a PLL. This is because for the shunt inverter, the power loop outputs are voltage amplitude (E) and frequency (ω), and therefore the microgrid system frequency information can be obtained from the shunt inverter control loop. Subsequently, phase angle ωt or $\int \omega dt$ used for the series inverter can be calculated using the system frequency obtained from the shunt inverter. Similarly, the fundamental frequency f_0 required for mean value calculation, as shown in Fig. 7(a), and ω for the controller in (4) can again be obtained from the shunt inverter control loop.

III. Limitation of Fault Currents During Utility Voltage Sags

With the aforementioned control schemes implemented, the quality of power in the microgrid and quality of current flowing between the microgrid and utility are significantly enhanced. These control schemes however need further fine-tuning to ensure satisfactory performance in the event of utility voltage sag. Referring to Fig. 9, which shows the voltage phasors at various nodes along the distribution feeder, $\vec{V}_D$ must be held relatively constant at its nominal value to prevent tripping of sensitive loads during the sag. This is achieved by disabling the external power control algorithms and setting the voltage references ($\{V_\alpha^*, V_\beta^*\}$ in Fig. 3) of shunt inverter A at, for an example, 90% of their desired nominal values with their phase-angles locked at the pre-sag values. Doing this however causes a large voltage difference($\Delta\ \vec{V}=\vec{V}_D - \vec{V}_{\rm sag}$) to appear across series inverter B and the distribution feeder, resulting in large fault currents flowing along the feeder. If these fault currents are allowed to flow through the line until clearance of the sag or opening of the electromechanical circuit breaker, there is a risk of damaging semiconductor devices in the inverters.

A possible solution to avoid this damaging situation and hence protect the system would be to sense the occurrence of a voltage sag, and immediately after which, control series inverter B to act like a virtual current-limiting inductor L_0. As the PCC can be located far away from the power compensator, detection of voltage sags can only be done locally by measuring the three-phase line currents. Upon the instantaneous current value of a phase exceeding a specified threshold I_T, series inverter B immediately responds by acting as a virtual inductor to limit the current flowing through $\{R_{\rm Line}, L_{\rm Line}\}$ and maintain $\vec{V}_E \approx \vec{V}_{\rm Sag}$. Since $\vec{V}_E \approx \vec{V}_{\rm Sag}$ during the sag, smooth recovery from a voltage sag can be ensured by sensing $\vec{V}_E$, which will rise with $\vec{V}_{\rm sag}$ back to its nominal value. After which, the current-limiting action of series inverter B can be inhibited, and the power algorithms of shunt inverter A can be restored.

For controlling the series inverter as a virtual inductor, this paper extends on the flux-model control concept reported in [9], [10], to develop an alternative flux-charge control algorithm (see Fig. 10) with improved performance and immunity to system parameter variations. For flux-model control, the feedback variable used is the inverter terminal flux, defined as $\Phi = \int V_C dt$, and its reference is calculated as $\Phi_{ref} = -L_0 i_{Line}$, where V_C and i_{Line} represent the filter capacitor voltage and inverter output current (equal to the line current if a 1:1 series transformer is used) of the series inverter. [Note from the reference flux expression that a negative sign is intentionally added to account for the drawing of i_{Line} as flowing out of the series inverter in Fig. 10(a)]. Subtracting the flux variable from its reference then produces the flux error, which is subsequently fed to the flux regulator, implemented using P+resonant compensator given in (4).

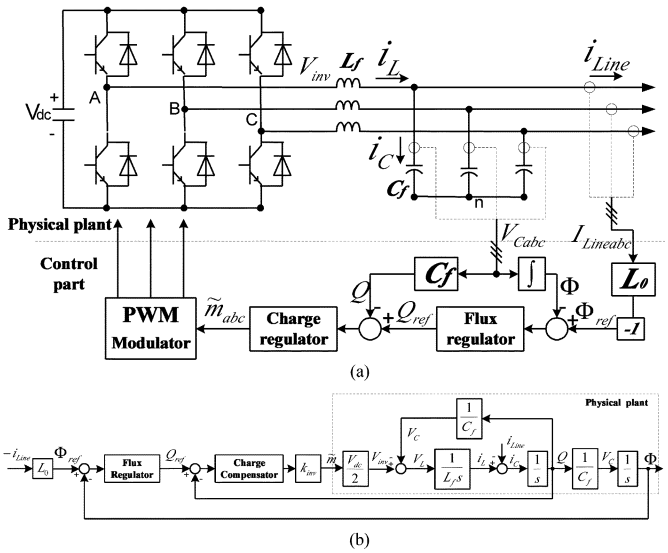


Fig. 10. Flux-charge control scheme of series inverter B (a) physical layout and (b) block diagram representation.

For a second-order LC filtered inverter, it can be shown through classical control analysis that the use of only flux-model will not effectively attenuate the resonant peak of the LC filter (details of the control analysis are not presented due to space limitation). To stabilize the system, an inner charge-model is proposed and embedded within the outer flux-model control loop. By duality, the charge control variable is defined as $Q = \int i_C dt = C_f V_C$, where i_C and C_f are the current and capacitance of the filter capacitor of the series inverter. This expression reveals that the Q variable can be calculated by simply multiplying C_f and V_C without requiring additional current sensor for measuring i_C and mathematical integration. The calculated charge variable is then subtracted from its reference $Q_{\rm ref}$ (output of the outer flux regulator) to give the charge error input to the inner charge regulator with a designed transfer function of $kT_d s \approx kT_d s/1 + (T_d s/N)$ (the added pole is to prevent noise amplification by limiting the regulator gain to Nk at high frequencies). The output signal from the charge regulator is finally passed to a PWM modulator (represented by $k_{\rm inv} = 2/V_{dc}$ for driving the physical inverter.

A feature of the proposed flux-charge-model control is its close similarity to the voltage-current control presented in Section II-A for shunt inverter A. Comparing the control diagrams in Figs. 3 and 10(b) reveals that flux-charge control in Fig. 10(b)

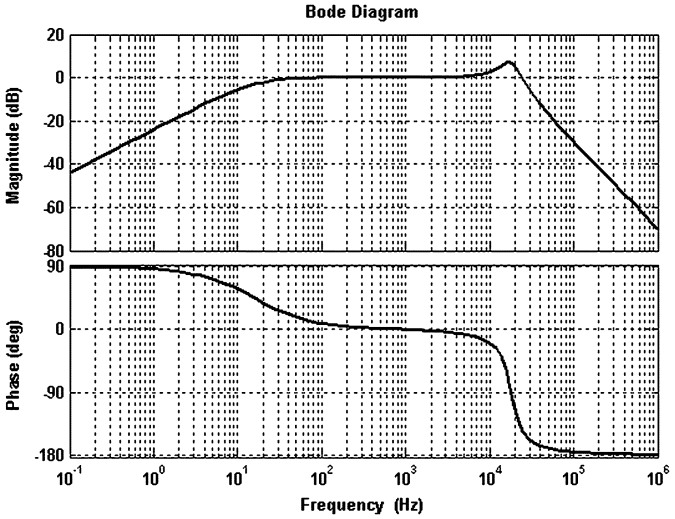


Fig. 11. Closed-loop bode plot of inner charge-model.

can be derived from the multiloop voltage-current control in Fig. 3 by integrating its input voltage and current variables. The only minor difference being the feeding back of the filter capacitor current, rather than the filter inductor current, for the flux-charge control, which as discussed earlier, simplifies the calculation of the charge variable. Progressing along the control path, the effects of input integration are subsequently nullified by the derivative term ($kT_d s$) found in the numerator of the charge regulator transfer function. Therefore, the proposed flux-charge control is expected to have the same closed-loop band-pass characteristics shown in Fig. 11 with $kT_d = 1000$ and $T_d/N = 0.00002$, for its inner charge-model as compared to the inner current loop of multiloop voltage-current feedback control (example bode plot for the inner capacitor current loop can be found in [11]). Also, the open-loop flux-charge-model transfer function in (11) and its corresponding open- and closed-loop bode plots in Fig. 12 with $2k_p = 0.08$ and $2k_i = 160$, are expected to exhibit good performance at the fundamental frequency with effective high frequency noise attenuation, similar to multiloop voltage-current control

$$
\begin{aligned}
G_{\Phi ol} &= \frac{2k_p kT_d s^2 + 2k_i kT_d s + 2k_p kT_d \omega_0^2}{a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \\
a_5 &= \frac{T_d}{N} C_f L_f; \quad a_4 = C_f L_f; \\
a_3 &= \frac{T_d}{N} + kT_d C_f + \frac{T_d}{N} C_f L_f \omega_0^2 \\
a_2 &= C_f L_f \omega_0^2 + 1; \quad a_1 = \omega_0^2 \left(\frac{T_d}{N} + kT_d C_f \right); \\
a_0 &= \omega_0^2. \qquad (11)
\end{aligned}
$$

A further criteria to note when designing the flux-charge-model concerns the selection of value for L_0. An appropriate value for L_0 would ensure the limiting of current within the specified threshold of I_T even under the worst voltage sag condition. The selection of L_0 should therefore begin by analyzing the worst case condition (case of largest $\Delta \vec{V}$ using the phasor diagram in Fig. 13, which shows the voltage phasors before and after an utility sag. Upon the occurrence of a sag, the PCC

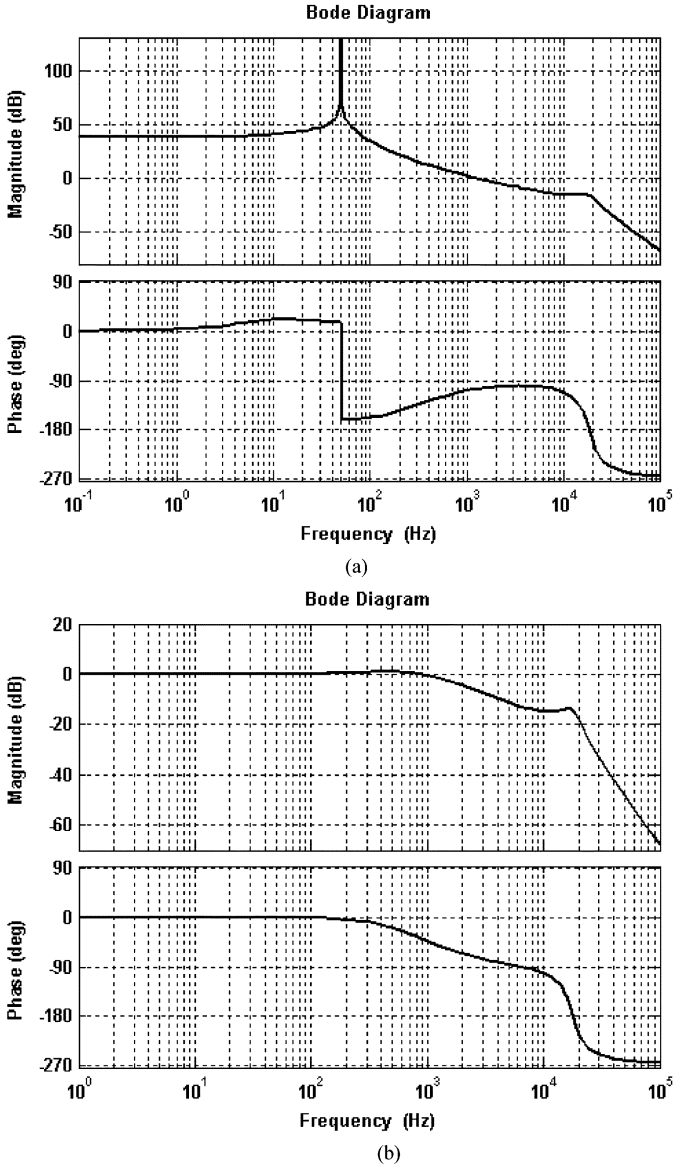


Fig. 12. Bode plots of the flux-charge-model control (a) open-loop and (b) closed-loop.

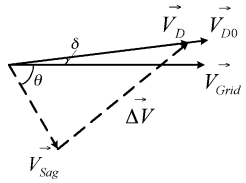


Fig. 13. Phasor diagram of sag condition.

voltage phasor changes from $\vec{V}_{\text{Grid}}$ (pre-sag) to $\vec{V}_{\text{Sag}}$ with a certain magnitude drop and a phase-angle jump θ. Instantly, the shunt inverter controlled voltage phasor changes from $\vec{V}_{D0}$ (pre-sag) to $\vec{V}_D$ with $\vec{V}_D = 0.9\vec{V}_{D0}$.

It is assumed that the worst-case sag condition for this study occurs when the utility voltage magnitude drops by 50% and $\theta = -60^\circ$, which is believed to be a typical worst-case scenario after considering cases reported in [12]. Assuming

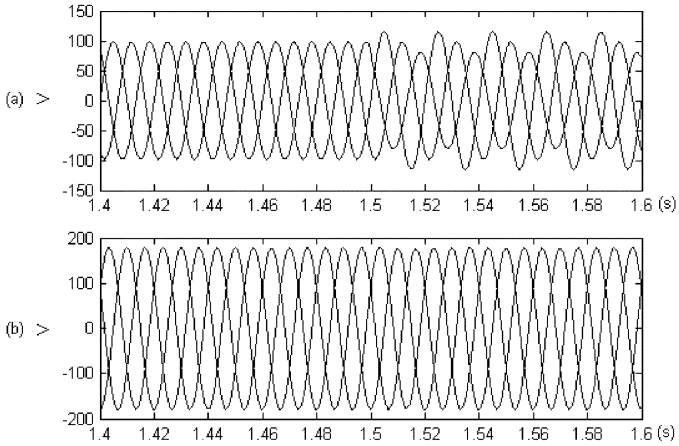


Fig. 14. Simulated (a) utility grid voltages and (b) sensitive load voltages in the microgrid.

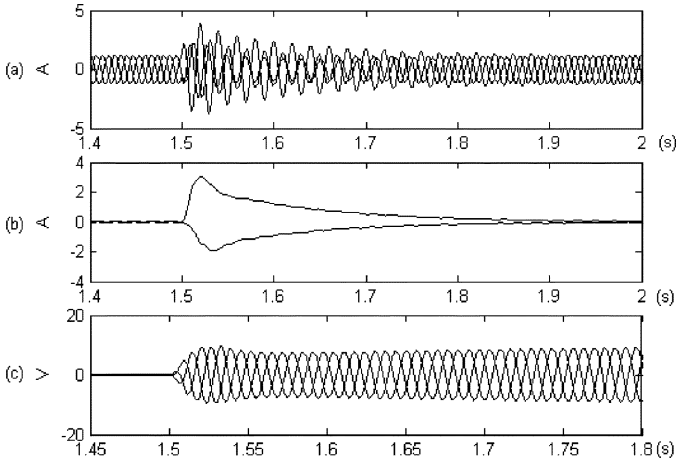


Fig. 15. Simulated (a) line currents, (b) negative-sequence line currents in the negative synchronous frame, and (c) filtered voltages generated by series inverter B.

further that θ is the angle between $\vec{V}_D$ and $\vec{V}_{\rm Sag}$ (since δ is usually small), and the magnitude of $\vec{V}_{D0}$ is nearly equal to that of $\vec{V}_{\rm Grid}$ (rated utility voltage E), the largest magnitude of $\Delta\vec{V}$ can be calculated as $|\Delta\vec{V}| = 0.78E$. The required L_0 can then be calculated using this limit, the given current limit I_T, line parameters $\{R_{\rm Line}, L_{\rm Line}\}$ and the expression $L_o = 1/\omega\sqrt{\Delta\vec{V}^2/I_T^2 - R_{\rm line}^2} - L_{\rm line}$.

IV. Simulation Results

Simulations using Matlab/Simulink have been carried out to test the effectiveness of the proposed compensator, as shown in Fig. 1. The system parameters used have been selected to represent those of typical distribution systems in [8], and are given in Table I (the transformer leakage resistance and inductance are lumped with $R_{\rm Line}$ and $L_{\rm Line}$, as mentioned in Section III). In addition, to emulate the digitally controlled experimental system implemented in Section V, simulations have been performed with zero-order-hold blocks of 100-μs sampling added to all feedback variables.

Fig. 14(a) and (b) show the utility and microgrid load voltages, respectively. Initially, the utility voltages are maintained balanced. At $t = 1.5$ s, they are intentionally made unbalanced by introducing 0.1 p.u. negative-sequence and 0.1 p.u. zero-sequence voltage components to the utility grid. This unbalance represents severer situation compared to those general scenarios reported in the literature [13]. With shunt inverter A in action, the load voltages in the microgrid are shown to be balanced throughout the simulated period, confirming the effect of inverter A in enhancing the quality of power in the microgrid. Similarly, with series inverter B added, the line currents are brought back to balanced condition with the negative-sequence current components gradually suppressed, as shown in Fig. 15(a) and (b). This balancing effect is achieved through proper injection of negative-sequence voltages (V_{Ca}, V_{Cb} and $V_{\rm Cc}$ in Fig. 1) by the series inverter from $t = 1.5$ s onwards, as shown in Fig. 15(c). To further confirm the proper functioning

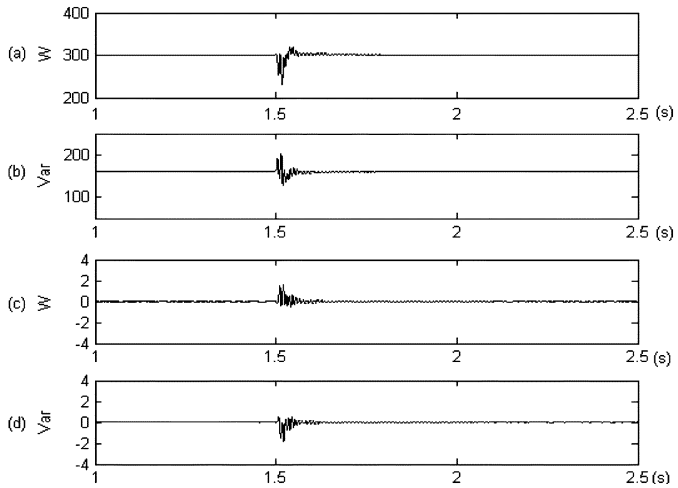


Fig. 16. Simulated (a) (b) real and reactive power supplied by shunt inverter A, and (c) (d) real and reactive power supplied by series inverter B.

of the proposed compensator, Fig. 16(a) and (b) show shunt inverter A dispatching the specified real power of 300 W and reactive power of 160 Var, while Fig. 16(c) and (d) show zero real and reactive power injection of series inverter B, as analyzed in Section III-B.

Another set of simulations has been carried out to test the performance of the compensator during an utility voltage sag. Fig. 17(a) shows the occurrence of an unbalanced utility voltage sag ($V_{\rm Ga} = 32\angle -44.7^\circ, V_{\rm Gb} = 66.4\angle -170^\circ$ and $V_{\rm Gc} = 54.5\angle 38.6^\circ$) at $t = 1$ s, while Fig. 17(b) shows the microgrid voltages being maintained at 90% of their desired nominal values by shunt inverter A during the sag (power control algorithms of inverter A are disabled during the sag, as mentioned in Section III). With the proposed current-limiting algorithm implemented, the series inverter acts like a large virtual inductor connected in series with the distribution feeder to limit the line currents below a specified threshold of $I_T = 6$ A instantaneously. The three-phase voltages across and line currents flowing through the series inverter are shown in Fig. 18(a) and

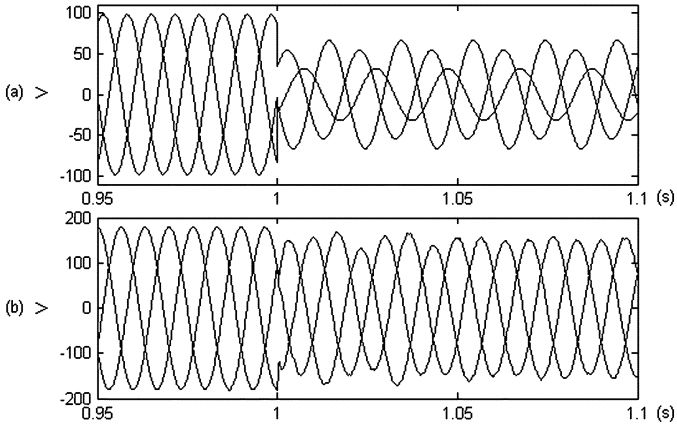


Fig. 17. Simulated (a) sag voltages at PCC and (b) sensitive load voltages in the microgrid.

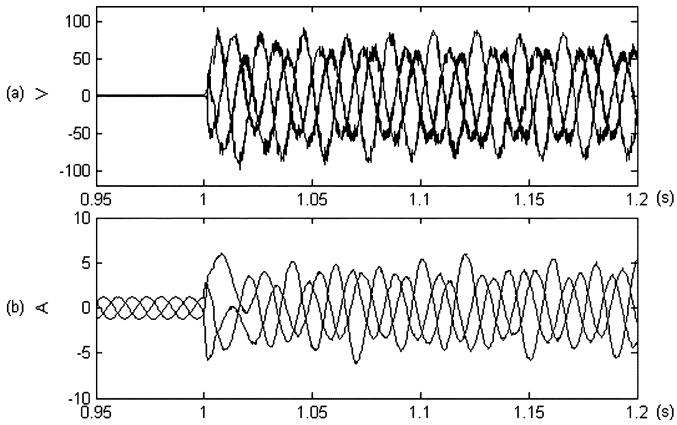


Fig. 18. Simulated (a) voltages injected by series inverter B and (b) line currents.

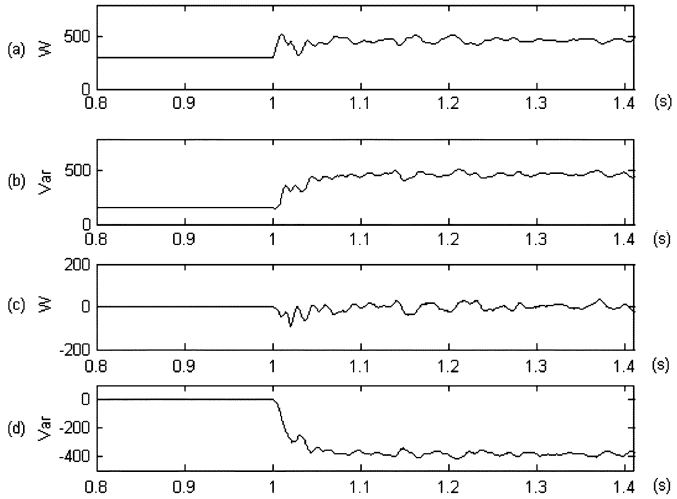


Fig. 19. Simulated (a) (b) real and reactive power supplied by shunt inverter A, and (c) (d) real and reactive power supplied by series inverter B.

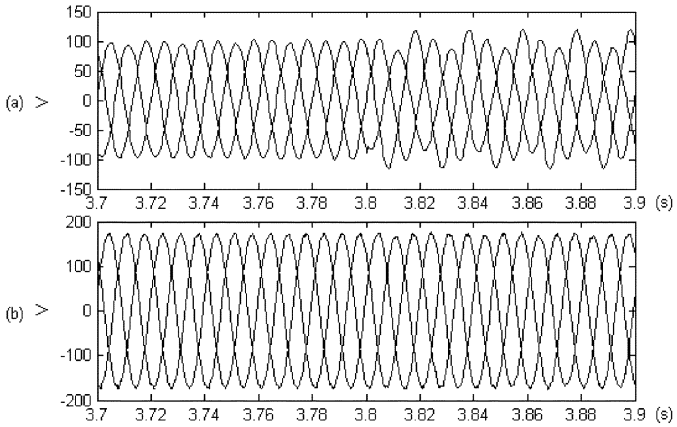


Fig. 20. Experimental (a) utility grid voltages and (b) sensitive load voltages in the microgrid.

(b) respectively. Last, Fig. 19(a) and (b) show the increase in real and reactive power supplied by the shunt inverter during the sag, while Fig. 19(c) and (d) show the real and reactive power absorbed by the series inverter. Note the (nearly) zero real power absorbed by the series inverter since it now functions like a fictitious inductor.

V. Experimental Verification

To verify the performance of the proposed compensator experimentally, a hardware prototype has been built in the laboratory using the same system parameters as in simulation (Table I). For the experimental system, a programmable ac source is used to represent the utility grid and is connected to an emulated microgrid through a three-phase back-to-back SCR isolation switch. The microgrid consists of the proposed compensator (a shunt IGBT inverter and a series IGBT inverter with an injection transformer), which is controlled using a dSPACE DS1103 controller card, and a connected RL load. To ensure proper starting of the experimental system, the utility and microgrid are powered up separately. After synchronizing the voltages at both ends of the SCR switch, the switch is closed to connect the microgrid and utility, allowing the system to transit smoothly into the grid-connected mode of operation.

Fig. 20(a) and (b) show the utility voltages and microgrid load voltages, respectively. At $t = 3.8$ s, the utility voltages become unbalanced with 0.1 p.u. negative-sequence and 0.1 p.u. zero-sequence voltage components added. Despite this unbalance in utility voltages, the load voltages in the microgrid are kept balanced by controlling shunt inverter A. Similarly, by controlling series inverter B, the currents flowing between the microgrid and utility grid can be balanced, as shown in Fig. 21(a). Other performance features such as the suppression of negative-sequence line currents and injection of negative-sequence voltages by series inverter B are shown in Fig. 21(b) and (c), respectively. Fig. 22(a)–(d) show the real and reactive power supplied by the shunt and series inverters. These figures clearly show the shunt inverter supplying its specified dispatched power of 300 W and 160 Var, and the series inverter injecting zero real and reactive power, as anticipated.

The compensator was also tested experimentally for its current-limiting function during utility voltage sags. Fig. 23(a) shows the occurrence of an utility voltage sag at $t = 1.2$ s (sag condition similar to that used for simulation). Fig. 23(b) shows the sensitive load voltages in the microgrid while it transits from normal to sag condition. Fig. 24(a) shows the series voltages

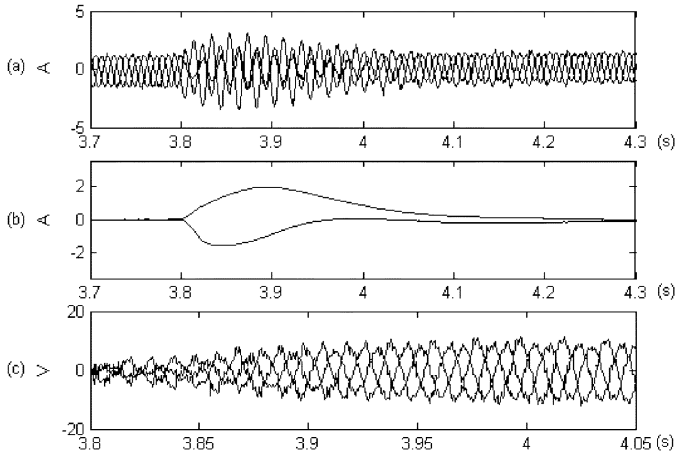


Fig. 21. Experimental (a) line currents, (b) negative-sequence line currents in the negative synchronous frame, and (c) filtered voltages generated by series inverter B.

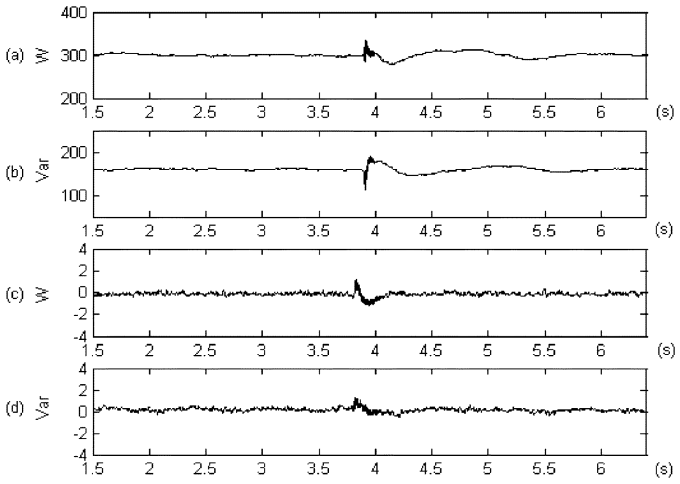


Fig. 22. Experimental (a) (b) real and reactive power supplied by shunt inverter A, and (c) (d) real and reactive power supplied by series inverter B.

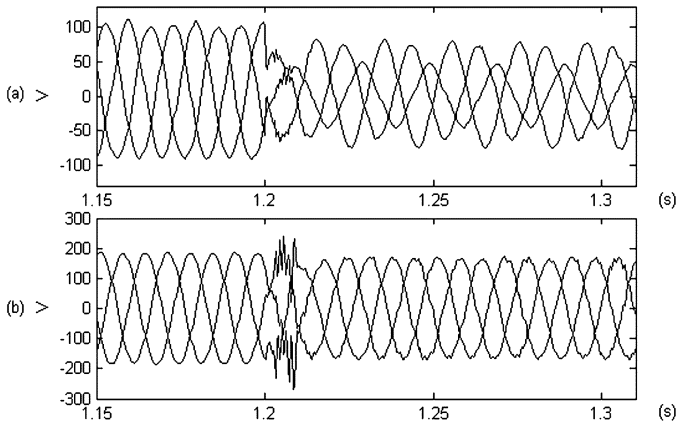


Fig. 23. Experimental (a) sag voltages at PCC and (b) sensitive load voltages in the microgrid.

generated by series inverter B, which now acts as a fictitious inductor. The corresponding limited line currents are shown in Fig. 24(b). Finally, Fig. 25(a) and (b) show the increase in real and reactive power supplied by the shunt inverter during the

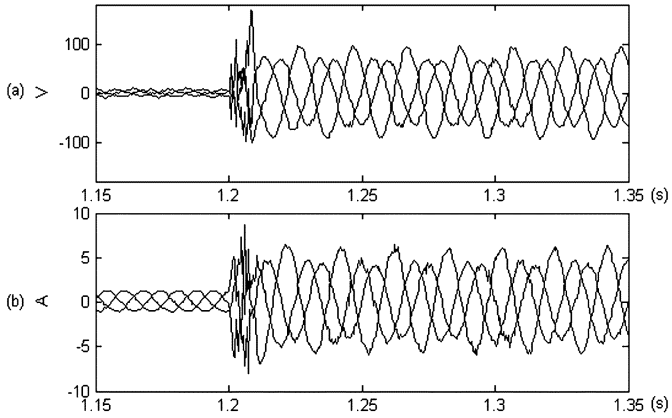


Fig. 24. Experimental (a) voltages injected by series inverter B and (b) line currents.

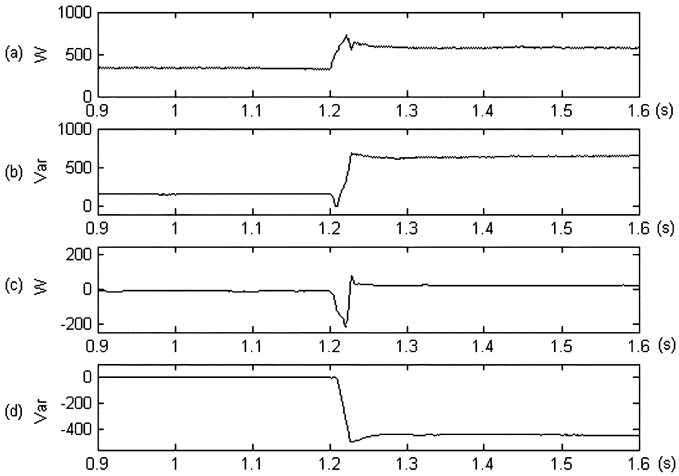


Fig. 25. Experimental (a) (b) real and reactive power supplied by shunt inverter A, and (c) (d) real and reactive power supplied by series inverter B.

sag, while Fig. 25(c) and (d) show the real and reactive power absorbed by the series inverter. Again, the real power absorbed by the series inverter is shown to be (nearly) zero.

VI. Conclusion

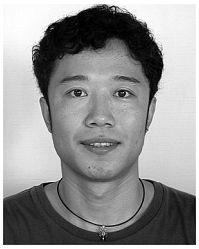
This paper proposes a new grid-interfacing power quality compensator to be used with individual DG systems in a microgrid. The compensator is implemented using shunt and series inverters with both inverters optimally controlled to enhance the power quality in the microgrid and the quality of currents flowing between the microgrid and utility. During the utility voltage sags, the series inverter can also be controlled to limit the flow of large fault currents, hence protecting equipment in the microgrid from serious damage. The practicality and effectiveness of the proposed compensator are verified by the simulation and experimental results.

References

[1] R. Lasseter, "Microgrids," in *Proc. Power Eng. Soc. Winter Meeting*, Jan. 27–31, 2002, pp. 305–308.

[2] A. von Jouanne and B. Banerjee, "Assessment of voltage unbalance," *IEEE Trans. Power Delivery*, vol. 16, no. 4, pp. 782–790, Oct. 2001.

[3] M. Prodanovic and T. C. Green, "Control and filter design of three-phase inverters for high power quality grid connection," *IEEE Trans. Power Electron*, vol. 18, no. 1, pp. 373–-380, Jan. 2003.
[4] Y. W. Li, D. M. Vilathgamuwa, and P. C. Loh, "Design, analysis and real-time testing of controllers for multi-bus microgrid system," *IEEE Trans. Power Electron*, vol. 19, no. 5, pp. 1195–-1204, Sep. 2004.
[5] C. B. Jacobina, M. B. deR. Correa, T. M. Oliveiro, A. M. N. Lima, and E. R. C. da Silva, "Current control of unbalanced electrical systems," *IEEE Trans. Ind. Electron*, vol. 48, no. 3, pp. 517–-525, Jun. 2001.
[6] D. N. Zmood, D. G. Holmes, and G. H. Bode, "Frequency-domain analysis of three-phase linear current regulators," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 601–-610, Mar/Apr. 2001.
[7] P. Mattavelli, "Synchronous-frame harmonic control for high-performance AC power supplies," *IEEE Trans. Ind. Appl.*, vol. 37, no. 3, pp. 864–872, May/Jun. 2001.
[8] P. Heine, A. Lehtonen, and E. Lakervi, "Voltage sag analysis taken into account in distribution network design," in *Proc. IEEE Power Tech. Conf.*, 2001, p. 6.
[9] H. Funato, T Ishikawa, and K. Kamiyama, "Transient response of three phase variable inductance realized by variable active-passive reactance (VAPAR)," in *Proc. IEEE APEC'01*, 2001, vol. 2, pp. 1281–1286.
[10] H. Funato, K. Kamiyama, and A. Kawamura, "Transient performance of power circuit including virtual inductance realized by fully digital controlled variable active-passive reactance (VAPAR)," in *Proc. IEEE PESC'00*, 2000, vol. 3, pp. 1195–1200.
[11] N. M. Abdel Rahim and J. E. Quaicoe, "Analysis and design of a multiple feedback loop control strategy for single-phase voltage-source UPS inverters," *IEEE Trans. Power Electron*, vol. 11, no. 4, pp. 532–541, Jul. 1996.
[12] M. H. J. Bollen, *Understanding Power Quality Problems: Voltage Sags and Interruptions*. New York: IEEE Press, 2000.
[13] R. C. Dugan, M. F. McGranaghan, and H. W. Beaty, *Electrical Power Systems Quality*. New York: McGraw-Hill, 1996.



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