A Single-Phase Single-Stage High Step-Up AC–DC Matrix Converter Based on Cockcroft–Walton Voltage Multiplier With PFC

Chung-Ming Young, *Member, IEEE*, Ming-Hui Chen, *Member, IEEE*, Shou-Heng Yeh, and Kuo-Hwei Yuo

***Abstract*—This paper proposes a high-performance transformerless single-stage high step-up ac–dc matrix converter based on Cockcroft–Walton (CW) voltage multiplier. Deploying a four-bidirectional-switch matrix converter between the ac source and CW circuit, the proposed converter provides high quality of line conditions, adjustable output voltage, and low output ripple. The matrix converter is operated with two independent frequencies. One of which is associated with power factor correction (PFC) control, and the other is used to set the output frequency of the matrix converter. Moreover, the relationship among the latter frequency, line frequency, and output ripple will be discussed. This paper adopts one-cycle control method to achieve PFC, and a commercial control IC associating with a preprogrammed complex programmable logic device is built as the system controller. The operation principle, control strategy, and design considerations of the proposed converter are all detailed in this paper. A 1.2-kV/500-W laboratory prototype of the proposed converter is built for test, measurement, and evaluation. At full-load condition, the measured power factor, the system efficiency, and the output ripple factor are 99.9%, 90.3%, and 0.3%, respectively. The experimental results demonstrate the high performance of the proposed converter and the validity for high step-up ac–dc applications.**

***Index Terms*—Cockcroft–Walton (CW) voltage multiplier, high step-up ac–dc converter, one-cycle control, power factor correction (PFC).**

I. Introduction

HIGH-VOLTAGE dc power supplies have widely applied to industries, science, medicine, military, such as test equipment, X-ray systems, dust-filtering, insulating test, and electrostatic coating [1]–[3]. Providing the advantages of high voltage ratio, low voltage stress on the diodes and capacitors, compactness, and cost efficiency, the conventional Cockcroft–Walton (CW) voltage multiplier is a popular option among high-voltage dc applications. As shown in Fig. 1, the well-known CW voltage multiplier is constructed by cascading a number of diode–capacitor stages with each stage containing two capacitors and two diodes. Theoretically, an n-stage CW voltage multiplier provides dc voltage with the value of $2n$ times of the magnitude of the ac voltage source under no-load condition. However, the dc output voltage is practically less than the theoretic value due to no-ideal characteristics of the circuit components [1], [3], [4]. Under heavy-load condition, the CW multiplier intrinsically presents not only poor output voltage regulation but also high output ripple with line frequency. In some applications, line-frequency transformers with high step-up ratio were generally used to cooperate with the CW voltage multiplier for higher voltage gain. However, sourced by the utility ac source, the transformers lead to inefficiency of bulk and cost, and the ripple problem still unsolved [5].

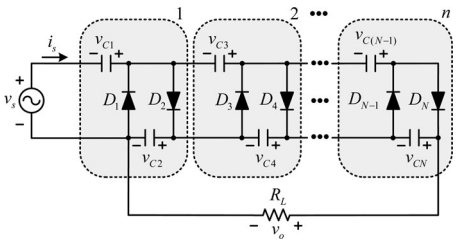

Fig. 1. Conventional n-stage CW voltage multiplier.

TAKING the advantages of the high-frequency switching technologies, many modified CW circuits have been developed for saving the volume of the transformers, smoothing the output ripple, and regulating the output voltage. In [6]–[8], some voltage-fed modified CW topologies, which provide not only high voltage gain but also simplicity of implementation, were proposed. Nevertheless, among these topologies, the high-frequency transformer with high turns ratios causes large winding capacitance and leakage inductance, which leads to high voltage and current stresses and higher switching losses on the switches. Moreover, operating in discontinuous conduction mode (DCM), these topologies incur more stress, losses, and electromagnetic interference (EMI) problems. In [9], series, parallel, and hybrid resonant converters incorporated with high-frequency and high step-up transformer were proposed to energize a CW circuit, in which the nonideal components of the transformer were under consideration. However, these converters were supplied only by dc sources. In [10]–[12], soft-switching techniques were applied to resonant-type CW circuits to reduce switching losses on power switches for enhancing the

Manuscript received May 10, 2011; revised December 2, 2011; accepted March 15, 2012. Date of current version July 13, 2012. This work was supported by the National Science Council of Taiwan under Project NSC 100-2221-E-011-009. Recommended for publication by Associate Editor K.-B. Lee.

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Digital Object Identifier 10.1109/TPEL.2012.2192450

system efficiency. In addition to these modified CW circuits, up to now, some cascaded single-switch step-up dc–dc converters without step-up transformer were also proposed in [13]–[15], which provided high voltage gain with advantages of simplicity and cost efficiency. However, capacitors of these topologies with higher voltage rating are needed when higher number of stages are deployed. In [15], a modified topology, with integrated multiphase boost converter and voltage multiplier, was proposed for high step-up conversion and high-power applications as well. In this topology, all capacitors in the voltage multiplier had identical voltage rating. Moreover, some nonisolated high step-up dc–dc converters with low-voltage dc input were proposed for renewable energy applications [16]–[19]. However, except sourced by dc power, such as photovoltaic generators, fuel cells, or batteries, these converters required a front stage for linking to the ac line. Some power factor correction (PFC) techniques have to apply to the front stage; otherwise, the converter will incur poor line quality. Some standards have been already available to improve this situation, such as IEC519, IEC555, and IEC1000-3-2 [20]–[22]. A lot of ac–dc converters with PFC techniques have been developed and applied into various types of electrical equipment [23]–[29]. In [23], the ac–dc topologies with high line quality were reviewed and classified, and most of them used hard-switching techniques. In [24] and [25], some modified boost PFC circuits with soft-switching techniques were proposed for enhancing the utilization of energy. However, only few of them were applied to high-voltage applications.

In [26], a two-stage structure cooperated with conventional CW circuit was proposed for high-voltage dc applications. Although providing good line condition and fast response, this topology demonstrated complexity and cost inefficiency. In [27], a single-stage transformerless topology integrated with a single-phase ac–ac converter and Dickson charge pump circuit was proposed for achieving high voltage gain and improving line conditions. Nevertheless, the voltage gain of this converter depended on duty cycles of switch current, capacitor current, the switching frequency, and switching load resistance. This led to complicated design considerations. Another topology with soft-switching technique, which consisted of a conventional single-phase boost ac–dc circuit, a four-switch full-bridge converter, a high step-up transformer, and a high-voltage rectifier, was proposed for high-voltage dc applications [28]. Applying PFC, this topology achieved high line quality, but efficiency and cost had to be considered for practical applications. In [29], a single-stage single-phase ac to high-voltage dc converter based on the CW voltage multiplier without step-up transformer was presented. Adding one boost inductor and one bidirectional switch to a conventional CW circuit, this converter provided simplicity, high efficiency, good line condition, and regulated dc output. Moreover, the control strategy for conventional single-switch boost ac–dc converter with PFC can be easily adopted for this converter. However, low ripple output still could not achieve by this structure.

A previous work on the proposed converter was conducted and presented in [30], in which a high step-up dc–dc converter based on CW voltage multiplier was discussed, i.e., the converter was energized by a dc source. In [30], four unidirectional switches formed the main converter and two independent switching frequencies were used to operate these switches. Successively, the unidirectional switches are replaced by bidirectional switches and the dc source is replaced by an ac source. By these replacements, the high step-up ac–dc converter proposed in this paper is shown in Fig. 2. The arrangement of the four bidirectional switches can be seen as a single-phase matrix converter deployed between the ac source and the CW circuit. With the help of the boost structure, in the proposed converter, not only the voltage gain can be higher than that of the conventional one but also the PFC technique can apply to the matrix converter to achieve high quality of line conditions and dc output regulation. In this paper, only continuous conduction mode (CCM) is discussed for its promising less stress, loss, and EMI problems. Moreover, the proposed converter deploys a single-phase matrix converter, which employs two independent frequencies. One of the frequencies applies to two of the four switches to perform PFC function, and the other applies to the rest of the two switches to determine the output frequency of the matrix converter. The latter frequency determines the output frequency of the matrix converter and, then, can be used to smooth the ripple voltage in the dc output. Even deploying bidirectional switches, the proposed converter can adopt PFC control methods of conventional ac–dc boost converters just with some modifications. Therefore, some commercial control ICs with PFC function can be easily applied to the proposed converter with an extra auxiliary circuit which modifies the original switching signal to trig the four bidirectional switches properly.

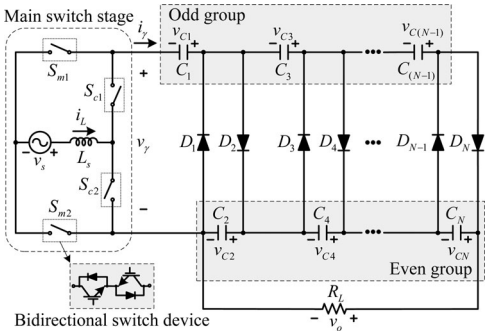


Fig. 2. Circuit configuration of the proposed converter.

In Section II, the circuit operation principle will be discussed and the steady-state voltage gain will be derived as well. Section III presents control and safe-commutation strategies of the proposed converter, and Section IV introduces the design considerations, in which output ripple will be discussed in detail. In Section V, a 1.2-kV/500-W prototype is built and the experimental results are displayed to verify the operation of the proposed converter. Finally, some conclusions are given in Section VI.

II. Steady-State Analysis

The proposed configuration is mainly composed of a single-phase matrix converter cascaded with a traditional *n*-stage CW voltage multiplier, as shown in Fig. 2. The single-phase matrix converter forms with four bidirectional switches that are divided

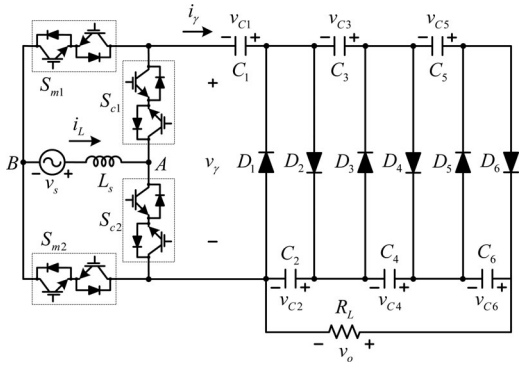


Fig. 3. Proposed converter with a three-stage CW voltage multiplier.

into two sets denoted as (S_{c1}, S_{c2}) and (S_{m1}, S_{m2}). The proposed converter is energized by a line-frequency ac source with a series inductor for boost operation. Till now, commercial products of bidirectional switches are not available [31]; thus, two antiseries insulated gate bipolar transistors with freewheel diode are used as a bidirectional switch in this paper.

A. Circuit Operation Principle

In order to simplify the analysis of circuit operation, a three-stage CW voltage multiplier is used in the proposed converter, as shown in Fig. 3. Before analyzing, some assumptions are made as follows:

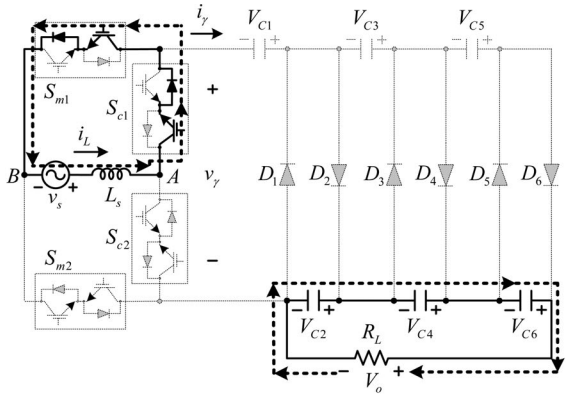
1) All of circuit elements are ideal and there is no power loss in the system.
2) All of the capacitors in the CW voltage multiplier are sufficiently large, and the voltage drop and ripple of each capacitor can be ignored under a reasonable load condition. Thus, the voltages across all capacitors are equal, except the first capacitor which voltage is one half of the others.
3) The proposed converter operates in CCM and under steady-state condition.
4) During demagnetizing period of the boost inductor, only one of the diodes in CW circuit will conduct. This phenomenon was discussed in [29].
5) To avoid the open-circuit of the inductor, a safe-commutation technique is practically used in the control strategy, which provides some overlap of the trig signals between S_{c1} and S_{c2}. Although this issue will be discussed Section III, analysis of circuit operation will ignore the safe-commutation states for simplicity.

According to the second assumption, each capacitor voltage in the CW voltage multiplier can be defined as

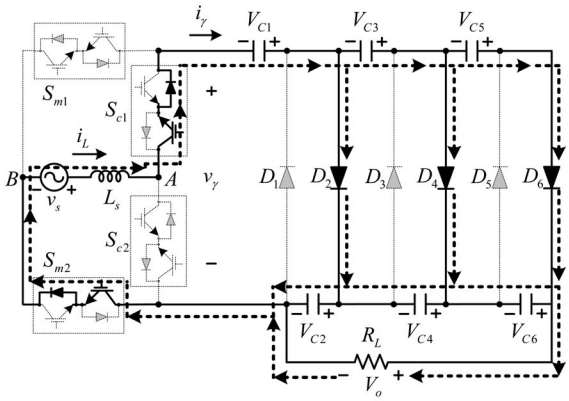
$$v_{Ck} = \begin{cases} V_C, & \text{for } k = 1 \\ 2V_C, & \text{for } k = 2, 3, \ldots, N \end{cases} \tag{1}$$

where v_{Ck} is the voltage of the kth capacitor, V_C is the maximum peak value of terminal voltage of the CW voltage multiplier under steady-state condition, and $N = 2n$.

For an n-stage CW voltage multiplier, the output voltage is equal to the total voltage of all even capacitors, which can be



(a)



(b)

Fig. 4. Circuit states and conducting paths of the proposed converter at mode I. (a) State 1. (b) State 2.

expressed as

$$V_o = NV_C \tag{2}$$

where V_o is the steady-state dc output voltage.

Substituting (2) into (1), each capacitor voltage can be rewritten as

$$v_{Ck} = \begin{cases} V_o/N, & \text{for } k = 1 \\ 2V_o/N, & \text{for } k = 2, 3, \ldots, N. \end{cases} \tag{3}$$

According to the polarity of the ac source and the switching state of S_{c1}, there are four operation modes of the proposed converter, denoted as modes I–IV. Moreover, combining with boost operation, each mode has two circuit states. Fig. 4 shows the two circuit states of mode I, which provides positive i_γ during positive-half cycle of the ac source, and Fig. 5 shows the two circuit states of mode II, which provides negative i_γ during negative-half cycle of the ac source. For simplicity, the circuit states of modes III and IV are not presented, and they can be obtained by changing the directions of i_γ and i_L from Figs. 4 and 5, respectively.

Obviously, S_{m1} and S_{m2} work as boost switches while S_{c1} and S_{c2} control the direction of i_γ, i.e., the output frequency of the matrix converter. Basically, S_{c1} (S_{m1}) and S_{c2} (S_{m2}) should be operated in complimentary mode and the

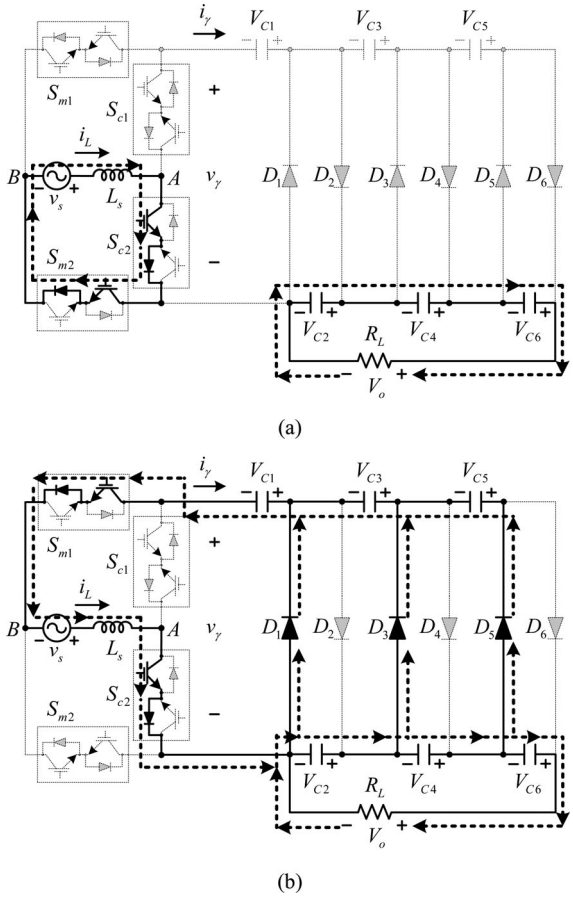


Fig. 5. Circuit states and conducting paths of the proposed converter at mode II. (a) State 1. (b) State 2.

operating frequencies of S_{c1} and S_{m1} are defined as f_c and f_m, respectively, where f_c is called alternating frequency and f_m is called modulation frequency.

For convenience, a simple case is used to explain the operation principle of the proposed converter. In this simple case, f_c is twice as large as line frequency and $f_m = 60$ kHz. Fig. 6(a) shows some selected waveforms including the trig signals for the four bidirectional switches. According to the trig signals of S_{c1} and S_{c2}, which are complementary with 50% duty, the four modes spread over a line cycle equally. A PFC control method is applied to the matrix converter, which will be detailed later; thus, the line current is nearly sinusoidal and in phase with the line source. In accordance with the timing of v_s and S_{c1}, the pulse-shape current i_γ has discontinuous sinusoidal envelops. The behavior between i_γ and CW circuit will be explained later in this section. Fig. 6(b) and (c) shows the zoom-in waveforms of i_L for modes I and II, respectively. The two states in modes I and II are related to the pulsewidth modulated (PWM) signals of S_{m1} and S_{m2}, and in state 2, $i_\gamma = \pm\, i_L$, where "+" is for mode I and "–" is for mode II. The circuit behavior in modes I and II will be given in the following:

1) *State 1 in mode I [see Fig. 4(a)]:* During DT_m interval, S_{m1} and S_{c1} are turned ON, the boost inductor is charged by the input source, i_γ is zero due to no current path, the even-group capacitors C_6, C_4, and C_2 supply to the load R_L, and the odd-group capacitors C_5, C_3, and C_1 are floating.
2) *State 2 in mode I [see Fig. 4(b)]:* During $(1 - D)T_m$ interval, S_{m2} and S_{c1} are turned ON, the boost inductor and input source transfer energy to the CW circuit by positive i_γ flowing through one of the even diodes [29]. The ON/OFF states of the diodes and charging behavior of the capacitors can be found in [29] as well.
3) *State 1 in mode II [see Fig. 5(a)]:* During DT_m interval, S_{m2} and S_{c2} are turned ON, the boost inductor is charged by the input source, i_γ is zero due to no current path, the even-group capacitors C_6, C_4, and C_2 supply to the load R_L, and the odd-group capacitors C_5, C_3, and C_1 are floating.
4) *State 2 in mode II [see Fig. 5(b)]:* During $(1 - D)T_m$ interval, S_{m1} and S_{c2} are turned ON, the boost inductor and input source transfer energy to the CW circuit by negative i_γ flowing through one of the odd diodes [29]. The ON/OFF states of the diodes and charging behavior of the capacitors can be found in [29] as well.

The circuit behaviors of modes III and IV can be obtained by similar processes but with opposite directions of both i_γ and i_L.

B. Derivation of the Ideal Static Voltage Gain

In this paper, the proposed converter is sourced by a sinusoidal voltage source, which can be expressed as

$$v_s = \sqrt{2} V_s \sin \omega_s t \tag{4}$$

where v_s is the line source, and V_s and ω_s are the rms value and angular frequency of v_s, respectively.

During state 1 in each mode, from Figs. 4(a) and 5(a), it can be seen that the voltage across nodes A and B is zero; thus, the current variation of i_L can be represented as

$$\Delta i_{L(\mathrm{on})} = \frac{v_s}{L_s} D T_m \tag{5}$$

where L_s is the boost inductor, D is the duty cycle of S_{m1} in modes I and III or the duty cycle of S_{m2} in modes II and IV, and $T_m = 1/f_m$ is the modulation period.

From Figs. 4(b) and 5(b) and (3), it can be seen that during state 2, the voltage across nodes A and B is equal to V_o /*N* both in modes I and II. Similarly, the terminal voltage V_{AB} is equal to $-V_o$ /*N* both in modes III and IV. Thus, the polarities of the terminal voltage V_{AB} in positive- and negative-half cycles have opposite sign. Consequently, the current variation of i_L can be represented as

$$\Delta i_{L(\mathrm{off})} = \frac{v_s - \mathrm{sign}(v_s) \cdot V_o/N}{L_s} (1 - D) T_m \tag{6}$$

where $\mathrm{sign}(v_s)$ denotes the sign of v_s.

From (5) and (6), the average inductor voltage over one modulation period T_m can be expressed as

$$L_s \frac{\Delta i_L}{T_m} = L_s \frac{\Delta i_{L(\mathrm{on})} + \Delta i_{L(\mathrm{off})}}{T_m} \tag{7}$$

where Δi_L is the variation of line current over one modulation period T_m.

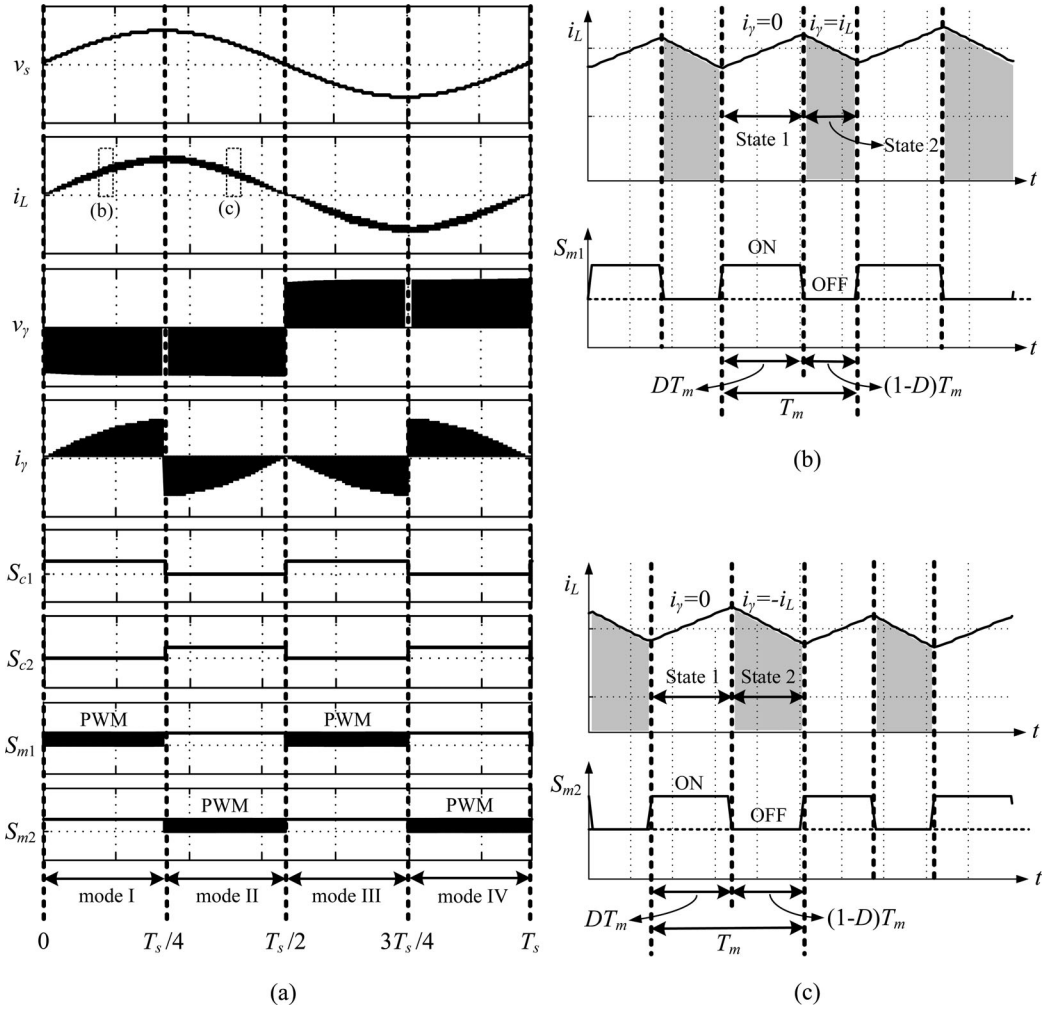


Fig. 6. Some selected waveforms of the proposed converter for illustrating operation modes. (a) Waveforms of v_s, i_L, v_γ, i_γ, and trig signals for $S_{m\,1}$, $S_{m\,2}$, $S_{c\,1}$, and $S_{c\,2}$. (b) Zoom-in waveforms of i_L and $S_{m\,1}$ at mode I. (c) Zoom-in waveforms of i_L and $S_{m\,2}$ at mode II.

If L_s is small enough, its influence on the low-frequency components of the converter waveforms is negligible [32], and the ideal static voltage gain of the proposed converter can be derived from (4)–(7)

$$M_V = \frac{V_o}{|v_s|} = \frac{N}{1-D} \tag{8}$$

where M_V is the ideal static voltage gain and $|v_s|$ is the absolute value of line source v_s.

Under suitable PFC control, the output voltage can be regulated as a constant dc value by adjusting D. According to (4) and (8), Fig. 7 shows the duty cycle varying within positive- or negative-half cycles of the line source v_s with different number of stages of CW circuit. For comparison, the corresponding duty cycle of a classic ac–dc boost converter with $V_o/\sqrt{2}V_s = 8$ is presented as well. It can be seen that with such high-gain requirement, the classic ac–dc boost converter almost operates with duty cycle higher than 0.875, which is not reasonable for practical application [33], while for the proposed converter, the duty cycles are in more reasonable regions.

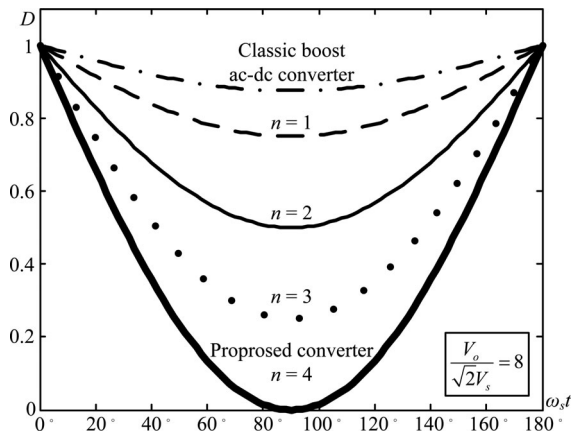


Fig. 7. Duty cycle varying within positive- or negative-half cycles of the line source v_s for the proposed converter with n = 1–4 and classic boost ac–dc converter.

III. Control Strategy

According to the circuit states shown in the previous section, the front stage of the proposed converter performs like a boost

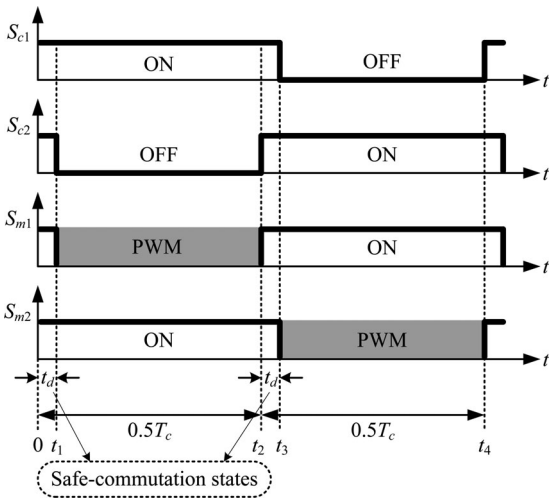


Fig. 8. Timing diagram of switching pattern for the proposed converter including safe-commutation states.

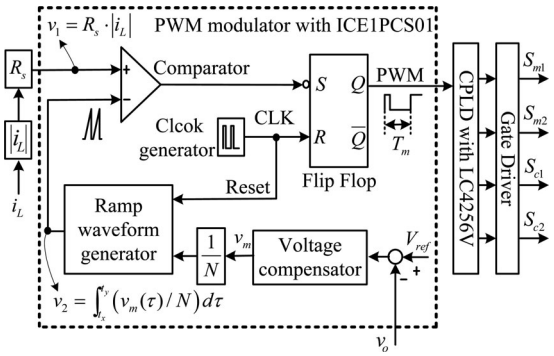


Fig. 9. Control scheme of the proposed converter.

converter, even deploying bidirectional switches. Thus, the proposed converter can adopt PFC control methods of conventional ac–dc boost converter with proper modifications. Consequently, some commercial control ICs with PFC function can be easily applied to the proposed converter with an extra auxiliary circuit that modifies the original switching signal to trig the four bidirectional switches properly.

Taking a close look at the circuit states in Figs. 4 and 5, it can be found that S_{c1} and S_{c2} (S_{m1} and S_{m2}) swap the conduction states at the changing instant between state 1 and state 2. If the commutation fails, the discontinuous inductor current will cause voltage spike and damage the switching elements. Therefore, the switching mechanism has to include some self-commutation strategies to deal with this concern. As shown in Fig. 8, the switching patterns of S_{c1} and S_{c2} (S_{m1} and S_{m2}) place a short overlap period to guarantee the self-commutation.

For facilitating design, this paper deploys ICE1PCS01 as the main controller for the PWM modulator, which adopts quasi-steady-state approach by using one-cycle control technique on leading-edge modulation, as shown in the left part of Fig. 9, in which the protective control devices are left out [34].

For the quasi-steady-state approach [35], the control aim is to provide a resistor emulator making the input current i_L to be proportional to the input line voltage v_s. Define the emulated resistance R_e as

$$R_e = \frac{v_s}{< i_L >} \tag{9}$$

where $\langle i_L \rangle$ is the average value of the input current over one modulation period T_m.

Substituting (8) into (9), the emulated resistance can be rewritten as

$$R_e = \frac{V_o \cdot (1-D)}{N \cdot |\langle i_L \rangle|}. \tag{10}$$

In general, R_e can be regulated by the following control law [35]:

$$R_s \cdot |\langle i_L \rangle| = \frac{v_m}{M_V} \tag{11}$$

where R_s is the equivalent current-sensing resistance and v_m is the modulation voltage determined by the error command and the compensator, as shown in Fig. 9. Substituting (8) into (11), we have

$$R_s \cdot |\langle i_L \rangle| = \frac{v_m \cdot (1-D)}{N}. \tag{12}$$

Then, according to (10) and (12), R_e can be represented as

$$R_e = \frac{R_s \cdot V_o}{v_m}. \tag{13}$$

It can be seen from (13) that if the modulation voltage v_m is controlled to be a constant, the emulated resistance R_e will be a constant resistance as well. Consequently, the input current will be proportional to the input line voltage as shown in (9). This control goal is implemented by adjusting the duty cycle to satisfy (12). For practical applications, the average inductor current can be approximately equal to the instant inductor current when the current ripple in the inductor is negligible during one modulation period [35]. Therefore, in this paper, the functions $v_1 = R_s \cdot |i_L|$ and $v_2 = \int_{t_x}^{t_y} (v_m(\tau)/N)\,d\tau$ are set to implement the control law, as shown in Fig. 9. Moreover, the PWM signal from ICE1PCS01 is fed into a complex programmable logic device (CPLD) LC4256V, as shown in the right part of Fig. 9. A timer established in the CPLD is used to set the period of T_c, i.e., the alternating frequency f_c. Also, a logical circuit programmed in the same CPLD modifies the PWM signal from ICE1PCS01 and then sends the modified signals to trig the four bidirectional switches. An overlap with interval t_d for self-commutation is implemented in the CPLD as well.

IV. Design Considerations

In this section, the current ripple in the line current is used to design the value of the boost inductor, and the output ripple voltage caused by both line frequency and alternating frequency is discussed, in which the relation between the size of the capacitors and the value of the ripple is derived and will be used to determine the value of the capacitance. Moreover, the voltage and current stresses on capacitors, switches, and diodes will be considered as well. Before designing, the system specifications of the prototype used in experiment is summarized in Table I.

TABLE I
SYSTEM SPECIFICATIONS OF THE PROTOTYPE

Output power, P_o	500W
Output voltage, V_o	1.2kV
Input line voltage, v_s	110Vrms
Line frequency, f_s	60Hz
Modulation frequency, f_m	60kHz
Alternating frequency, f_c	60Hz~1920Hz
Resistive load, R_L	2.88kΩ
Stage number, n	3

A. Boost Inductor Design

Generally, the maximum peak-to-peak ripple of the line current is used to design the value of the boost inductor, where the maximum peak current of the line current $I_{L,\max}$ occurs when $v_s = \sqrt{2}V_s$, and can be derived as

$$I_{L,\max} = \frac{\sqrt{2} \cdot P_o \cdot (1 + K_{\text{over}})}{\eta \cdot V_s} \tag{14}$$

where P_o is the rated output power, η is the efficiency at rated power, and K_{over} is the proportion factor of the overload. Under $P_o = 500\,\text{W}$ and $V_s = 110\ \text{V}_{\text{rms}}$, if $\eta = 0.9$ and $K_{\text{over}} = 0.1$, then $I_{L,\max} \approx 7.86\,\text{A}$.

Similarly, the minimum duty cycle $D_{\min}$ occurs when $v_s = \sqrt{2}V_s$, and the corresponding duty cycle $D_{\min}$ can be calculated from (8)

$$D_{\min} = \frac{V_o/N - \sqrt{2} \cdot V_s}{V_o/N} \approx 0.222. \tag{15}$$

Then, the minimum turn-on time can be estimated by

$$t_{\text{on,min}} = \frac{D_{\min}}{f_s} = 3.7\ \mu\text{s}. \tag{16}$$

If the expecting percentage of the maximum peak-to-peak ripple of the line current K_I is set below 5%, then from (14) to (16), the value of the inductance must be fit the following:

$$L_s \geq \frac{\sqrt{2} \cdot V_s \cdot t_{\text{on,min}}}{K_I \cdot I_{L,\max}} = 1.46\,\text{mH}. \tag{17}$$

This result can be used to determine the value of the boost inductor, and $L_s = 1.5$ mH is used in the experiment.

B. Determination of the Capacitance

The dc output ripple of the proposed converter is used as a criterion to design the value of the capacitance in the CW voltage multiplier. Corresponding to the output and input frequencies of the matrix converter, i.e., f_c and f_s, the dc output ripple consists of two main components: one is caused by f_c and the other one is caused by f_s. The former ripple component can be analyzed by current-fed mode analytical principle [36]. From [36], the ripple corresponding to the alternating frequency can be derived as

$$\delta V_{o,fc} = \sum_{i=2,4,\ldots}^{2n} \frac{I_o}{f_c C} \left(\frac{2n - i + 1}{2} \right) \tag{18}$$

where I_o is the average load current, C is the value of the capacitance, and all capacitors are identical. Because PFC is a control goal of the proposed converter, it is assumed that unity power factor is achieved at the ac side. Consequently, for a single-phase system, the instantaneous power with $2f_s$ pulsating frequency will reflect to the dc output side and cause ripple component with same frequency. Ignoring the energy stored in the inductor, the latter ripple component caused by f_s can be obtained approximately as

$$\delta V_{o,2\,fs} \approx \frac{n \cdot I_o}{2\omega_s \cdot C} \tag{19}$$

where $\omega_s = 2\pi f_s$ and f_s is the line frequency.

It has to mention that (19) demonstrates the worst scenario of the ripple caused by f_s, which occurs when the rightmost diode is conducting in the whole positive-half cycle of input line voltage. For verification, a simulation is conducted with $V_s = 110\,\text{V}$, $V_o = 1200\,\text{V}$, $P_o = 500\,\text{W}$, $f_s = 60\,\text{Hz}$, and $f_c = 960\,\text{Hz}$. Fig. 10 shows the simulation results including the total ripple, the ripple component caused by f_s, and the ripple component caused by f_c. It can be seen that the waveform of $\delta v_{o,2fs}$ is similar to the traditional diode bridge rectifier, while $\delta v_{o,fc}$ is strongly dependent on i_γ which is clearly with alternating frequency f_c. Thus, the behaviors of the two ripple components agree with the previous analysis.

For distinguishing these two ripple components further, the values of these two ripples versus the values of the alternating

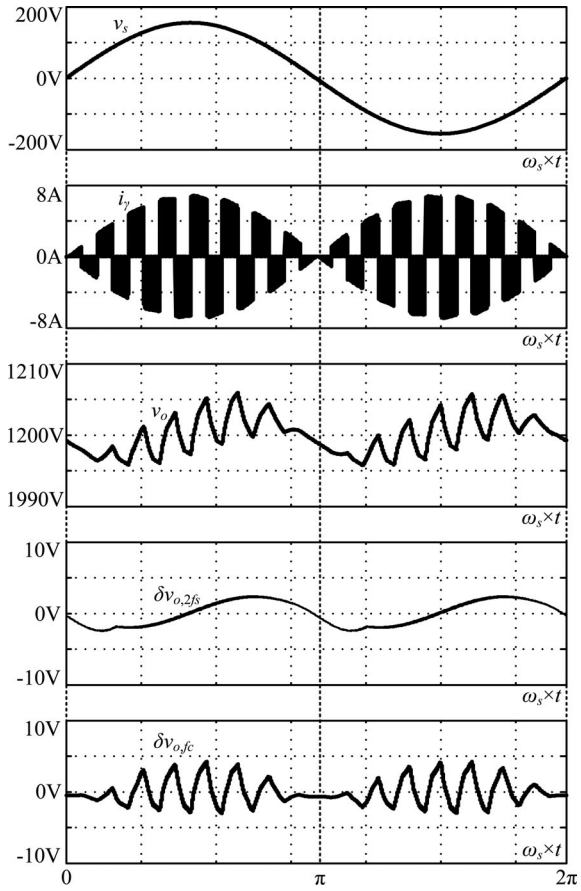


Fig. 10. Simulated waveforms of v_s, i_γ, v_o, v_o, $\delta v_{o,2fs}$, and $\delta v_{o,fc}$ with $f_c = 960\,\text{Hz}$ and $P_o = 500\,\text{W}$.

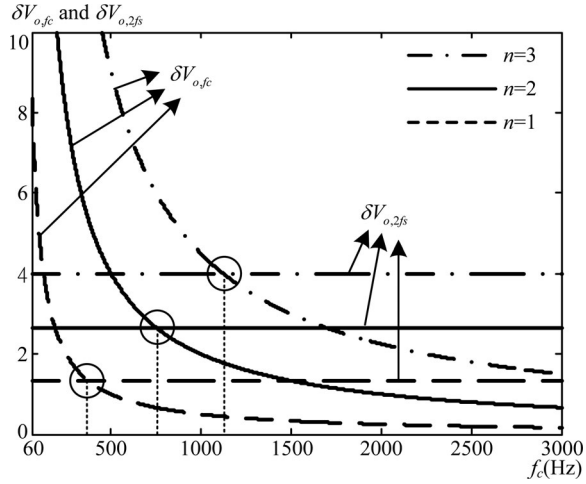


Fig. 11. Normalized output voltage ripple versus alternating frequency with different stages of CW circuit.

frequency are shown in Fig. 11. For convenience, the data presented in Fig. 11 are obtained by normalizing I_o(mA)/$C(\mu\text{F}) = 1$, and three different stages of CW circuit are considered. Obviously, both $\delta V_{o,2fs}$ and $\delta V_{o,fc}$ are proportional to the number of the stages, while $\delta V_{o,fc}$ is antiproportional to f_c. From the intersections of two corresponding ripple curves marked with the circles in Fig. 11, it is easy to distinguish which component dominate the ripple behavior and what alternating frequency should be chosen to meet the desired ripple voltage.

The peak-to-peak output ripple of the proposed converter is difficult to derive a complete equation, because the ripple voltage is the interaction of two components with two independent frequencies. However, the worst case of peak-to-peak ripple can be obtained by directly summing the two individual peak-to-peak ripple components, which can be represented as

$$\delta V_o = \delta V_{o,2fs} + \delta V_{o,fc}. \tag{20}$$

Consequently, according to (18)–(20), the value of the capacitance can be derived as

$$C \geq \frac{n \cdot I_o}{K_{\text{RF}} \cdot V_o} \left(\frac{n \cdot \omega_s + f_c}{2 f_c \cdot \omega_s} \right) \tag{21}$$

where $K_{\text{RF}} = \delta V_o / V_o$ is the desired ripple factor. If K_{RF} is set below 10% and the proposed converter is operated at $f_c = 60$–1960 Hz, then according to (21), the value of the capacitance must be higher than 274 μF. In this paper, the capacitors with $C = 470$ μF are used in the experiment.

C. Capacitor Voltage Stress

To simplify the determination of capacitor voltage stress, the voltage drop on each capacitor is ignored. Then, according to (3), the maximum voltage stress on each capacitor can be approximated to

$$V_{Ck,\max} = \begin{cases} V_{o,\max}/N, & \text{for } k = 1 \\ 2V_{o,\max}/N, & \text{for } k = 2, ..., N \end{cases} \tag{22}$$

where $V_{o,\max}$ is the maximum value of output voltage, and $V_{Ck,\max}$ is the maximum value of the voltage across the kth capacitor. From (8) and (22), it can be seen that the capacitor voltage of the proposed converter is not dependent on the number of the cascade stages. According to (22), if $K_{\text{RF}} = 10\%$, i.e., $\delta V_o = 120$ V, then $V_{o,\max} = 1260$ V and $2V_{o,\max}/N = 420$ V. In the experiment, the same voltage ratings with 500 V for all capacitors are chosen.

TABLE II
COMPONENTS LIST FOR THE PROTOTYPE

Components Description	Symbol	Value/Part no.
Control IC	-	ICE1PCS01
CPLD	-	LC4256V
Boost inductor	L_s	1.5mH
Power switches	S_{m1}, S_{m2}, S_{c1}, S_{c2}	IXGH30N60C3D1
Capacitors	$C_1 \sim C_6$	470μF/500V
Diodes	$D_1 \sim D_6$	SF20L60U
Gate driver	-	HCPL-3120

D. Switch Voltage and Current Stress

According to the circuit operation principle detailed in Section II, the maximum current and voltage stresses of each switch in the proposed converter are $V_{o,\max}/N = 210$ V and $I_{L,\max} \approx 7.86$ A, respectively.

E. Diode Voltage and Current Stress

Similarly, according to Section II, the maximum voltage and current stress on the diodes in the proposed converter are $2V_{o,\max}/N = 420$ V and $I_{L,\max} \approx 7.86$ A, respectively. Although the voltage stresses of the diodes are twice as large as of the switches, they are not dependent on the number of the cascade stages.

V. EXPERIMENTAL RESULTS

For demonstrating the correction and the validity of the proposed converter, a 1.2-kV/500-W prototype was built for test and measurement. A commercial IC (ICE1PCS01) was deployed as the PFC controller which generated the original PWM signal. A CPLD (LC4256V) modified the PWM signal and then sent to the matrix converter which was formed by four bidirectional switches. A timer established in the CPLD was used to set the period of T_c. Finally, a three-stage CW voltage multiplier was connected to the output of the matrix converter. According to design considerations, the system specifications and the components used in the experiment are summarized in Tables I and II, respectively.

For comparison, a conventional three-stage voltage source CW multiplier with the identical output voltage and power was built, tested, and measured. An ac source with 183 V_{rms} was supplied to the conventional CW circuit, i.e., the voltage conversion ratio is $V_o/\sqrt{2}V_s = 4.64$. The voltage gain of the proposed converter is $V_o/\sqrt{2}V_s = 7.71$, which is higher than the conventional one under the same output voltage. Fig. 12 shows the experimental waveforms of the conventional CW circuit and the proposed converter with $f_c = 60$, 960, and 1920 Hz, respectively. From Fig. 12, the conventional CW circuit incurs high distorted

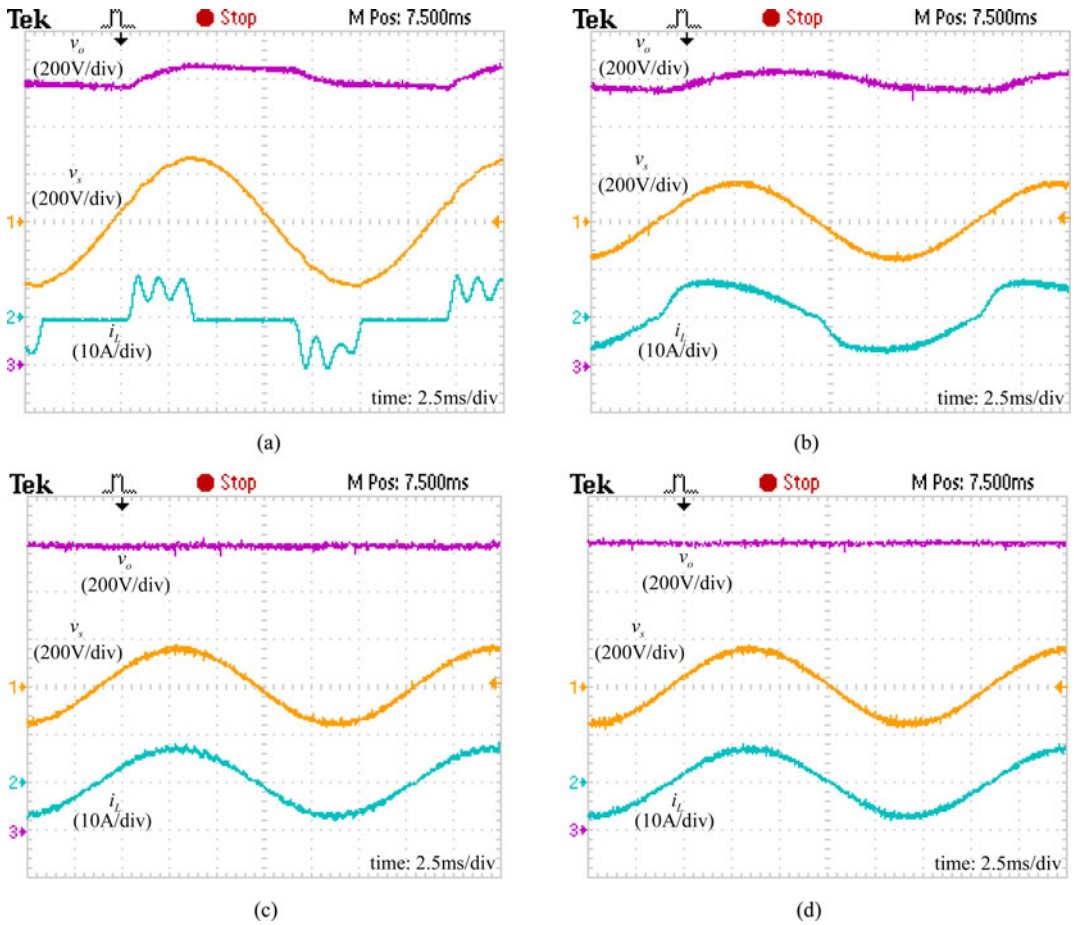


Fig. 12. Experimental waveforms of v_s, i_L, and v_o at full-load condition. (a) Conventional CW circuit. (b)–(d) Proposed converter with f_c = 60, 960, and 1920 Hz, respectively.

line current, poor power factor (68%), and high output ripple, while the proposed converter provides significantly good line conditions and rather low output ripple except in the case of f_c = 60 Hz. The reason of the distorted line current in Fig. 12(b) is that alternating frequency dominates the output ripple when low f_c is set for operation. Consequently, the high-ripple output affects the control low used in the one-cycle PFC controller, as shown in (13).

For further comparison, Table III summarizes the characteristic of the line currents for the experimental cases. From Table III, the line current of the conventional case contains both significantly odd harmonics and even harmonics. Thus, the line current is not only highly distorted but also half-wave asymmetric. However, the line currents are significantly improved for the proposed converter with f_c = 960 and 1920 Hz, respectively.

For evaluating the dc-side performance, Fig. 13 shows the waveforms of i_γ and ripple voltage associated with v_s for the proposed converter. From Fig. 13, it can be seen that with increasing alternating frequency, the output ripple decreases from 79.2 V for f_c = 60 Hz to 10.8 V and 8.4 V for f_c = 960 Hz and 1920 Hz, respectively. According to the experimental waveforms in Figs. 12 and 13, the function of the proposed converter agrees well with the theoretical analysis.

TABLE III
MEASURED LINE CURRENT HARMONICS FOR EXPERIMENTAL RESULTS

	CW circuit	Proposed converter		
THD_i (%)	74.81	f_c = 60Hz	f_c = 960Hz	f_c = 1920Hz
		14.14	3.73	2.60
Harmonic order (h)	A_h / A_1 (%)			
2	12.88	1.13	0.54	0.80
3	57.93	11.61	1.31	1.50
4	10.16	0.44	0.18	0.10
5	7.28	6.51	0.90	0.90
6	6.69	0.28	0.14	0.32
7	17.93	3.67	0.46	0.34
8	15.44	0.20	0.20	0.31
9	11.93	2.30	0.50	0.44
10	8.05	0.46	0.18	0.30
11	3.77	0.88	0.44	0.45
12	13.79	0.33	0.05	0.13
13	9.38	0.57	0.57	0.44
14	21.58	0.11	0.14	0.10
15	3.93	0.22	0.38	0.29
16	13.76	0.24	0.20	0.23
17	0.78	0.16	0.76	0.49
18	5.74	0.07	0.59	0.18
19	1.08	0.15	0.40	0.31
20	6.59	0.15	0.17	0.16

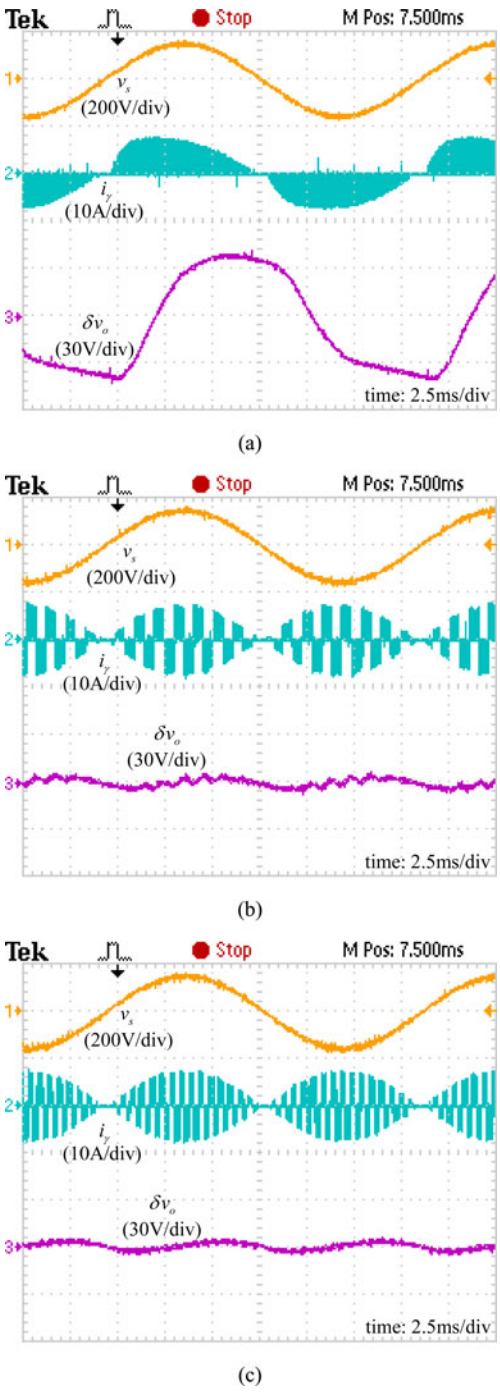


Fig. 13. Experimental waveforms of v_s, i_γ, and δv_o at full-load condition. (a) $f_c = 60$ Hz. (b) $f_c = 960$ Hz. (c) $f_c = 1920$ Hz.

Figs. 14 and 15 show the measured efficiency, power factor, and total harmonic distortion (THD_i) both for the conventional CW and the proposed circuits over the full power range. As shown in Fig. 14, although the conventional circuit provides very high efficiency, the poor power factor and THD_i lead to heavy burden on the main source. Although the efficiency of the proposed converter, as shown in Fig. 15(a), cannot compete with its counterpart due to the extra losses in the matrix converter, it still can be accepted by most applications. Moreover, as shown

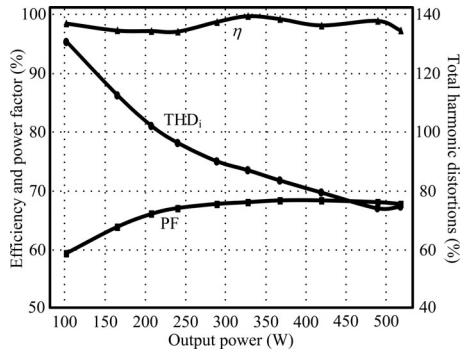


Fig. 14. Experimental results of efficiency, power factor, and THD of the conventional CW circuit under different load conditions.

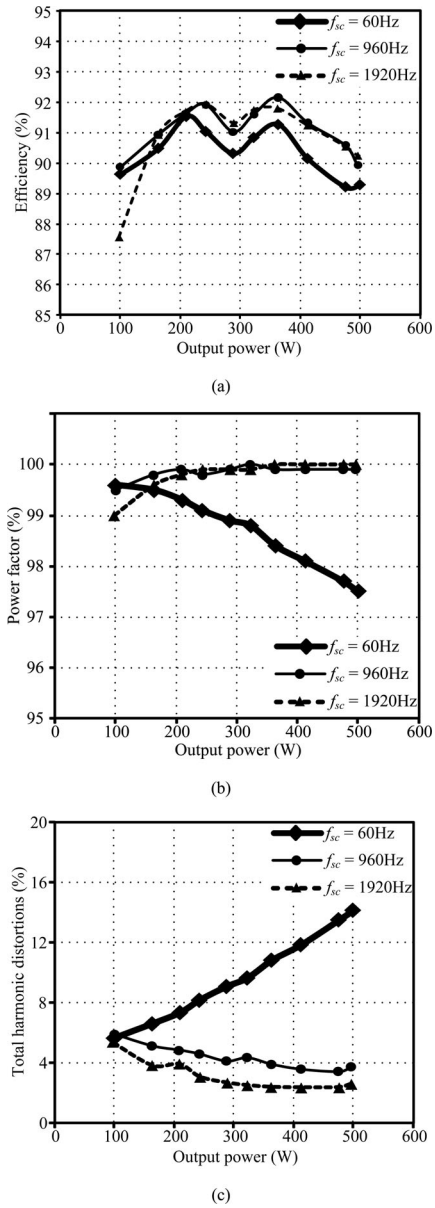


Fig. 15. Experimental results of the proposed converter with different f_c and different load conditions. (a) Efficiency. (b) Power factor. (c) THD.

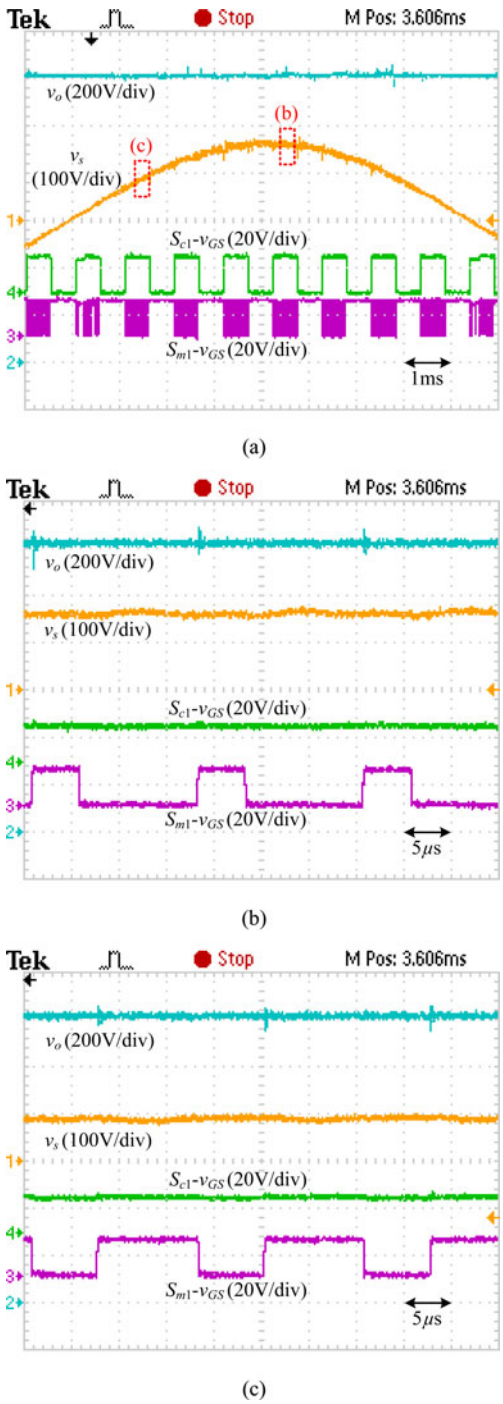


Fig. 16. (a) Experimental waveforms of v_o, v_s, S_{c1}-v_{GS}, and S_{m1}-v_{GS} when $P_o = 400$ W, $V_s = 110$ V_{rms}, $V_o = 1.2$ kV, and $f_c = 960$ Hz during positive-half cycle of input line source. (b) Zoom-in waveforms of area b ($v_s = 155$ V). (c) Zoom-in waveforms of area c ($v_s = 80$ V).

in Fig. 15(b) and (c), the proposed converter provides well performances of power factor and THD which are now required by more and more standards.

Finally, Fig. 16(a) shows the experimental waveforms of v_o, v_s, S_{c1}-v_{GS} and S_{m1}-v_{GS} when $P_o = 400$ W, $V_s = 110$ V_{rms}, $V_o = 1.2$ kV, and $f_c = 960$ Hz during positive-half cycle of line source. Obviously, the output voltage is regulated at 1.2 kV with rather small ripple. Moreover, Fig. 16(b) and (c) shows corresponding zoom-in waveforms of the two marked areas in Fig. 16(a), respectively. As shown in Fig. 16(b) and (c), the duty cycles are equal to 0.287 and 0.609 corresponding to $v_s = 155$ V [area (b)] and $v_s = 80$ V [area (c)]. On the other hand, by (8), the theoretical duty cycles can be calculated, i.e., $D = 0.225$ and $D = 0.6$ corresponding to the same instantaneous values of v_s. Compared with experimental and theoretical results, it can be found that the duty cycles have a little difference due to some nonideal characteristics of components. However, these results still can prove the correctness of the ideal voltage gain as given in (8).

VI. Conclusion

In this paper, a single-phase single-stage high step-up ac–dc matrix converter based on CW voltage multiplier is proposed. The four-bidirectional-switch matrix converter operated at two independent frequencies f_m and f_c. The former frequency is associated with PFC control, while the latter frequency can be used to smooth the output ripple. The operation principle, control strategy, and design considerations of the proposed converter were analyzed and discussed in this paper. Moreover, how line frequency and alternating frequency influenced the amplitude of the output ripple was discussed and some design criteria were given as well. For convenience, the PFC was achieved by adopting a commercial control IC associating with a CPLD. A 1.2-kV/500-W laboratory prototype of the proposed converter was built for test, measurement, and evaluation. The experimental results demonstrated the high performance of the proposed converter and the validity for high step-up ac–dc applications. The strategy of various alternating frequencies which can smooth the ripple further will be conducted in the near future. Finally, the precise derivation of voltage drop of the proposed converter will also be conducted for completing the steady-state analysis.

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