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An energy optimized control scheme for a transformerless DVR

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ABSTRACT

The dynamic voltage restorer (DVR) is considered as the most effective and economic solution for voltage disturbances. This paper presents an energy optimized control scheme for a transformerless DVR. The DVR structure is based on a cascaded H-bridge multilevel inverter topology to eliminate the need of insertion transformers. The proposed control algorithm maintains a balanced load-side voltage even during the compensation of unbalanced disturbances with a minimum active power injection. Moreover, the proposed scheme maximizes the ride-though capability of the DVR during voltage sags. This feature is verified by using capacitors instead of dc sources as energy storage elements for the DVR. Furthermore, the proposed minimum energy scheme prevents the rise in the dc-side voltage of the inverter when compensating voltage swells. The performance of the proposed DVR system is evaluated for compensating different types of voltage disturbances. The results validate the robustness and the accuracy of the proposed system.

1. Introduction

Voltage disturbances such as sags, swells, and flickers are the most common power quality problems. The effects of these disturbances range from minor annoyance up to the complete shutdown of the entire production process [1]. To reduce the economic impact of voltage disturbances, many solutions for protecting sensitive loads such as uninterruptible power supplies (UPSs) and dynamic voltage restorers (DVRs) are proposed. The UPS provides a complete protection against all power quality disturbances; however, it is associated with large fixed and operating costs especially if the UPS is to be installed in the medium voltage level. The DVR provides a cost effective solution to voltage quality disturbances. It injects a compensating voltage in series with the source-side voltage so that the load-side voltage remains undisturbed.

The DVR system configurations differ in the used inverter technology, the energy storage element, and the circuit topology. The most common inverters are the three-phase inverter, three single-phase inverters, and multilevel inverters (MLI). Numerous storage element systems can be used in the DVR such as batteries [2], capacitors [3,4], superconducting magnetic energy storage (SMES) [5], and flywheel [6]. Different DVR circuit topologies are discussed in [7].

There are many control strategies for the DVR [8]. The pre-fault method is the basic compensation technique as the disturbance is cleared and the load voltage is kept at its pre-fault value. The main drawback of this method is the large active power supplied by the DVR during compensation [9]. Another control strategy is the post-fault method which is based on constructing a three-phase balanced voltage from the extracted disturbance. This control strategy can achieve either minimum voltage or minimum energy DVR operation. There are two techniques to realize this method; the first technique is based on using the phase-locked loop (PLL) [10], while the second is based on the symmetrical components [11].

A transformerless DVR based on 9-level cascaded H-bridge topology is presented in this paper. Using multilevel inverter topology improves the maximum voltage injection ability of the DVR. In addition, the DVR can be used in medium voltage networks directly without the insertion transformer. The elimination of the insertion transformer reduces both cost and size of the DVR. Problems related to the transformer such as the saturation and the phase shift are avoided [12]. Furthermore, the MLIs have high number of switching states so that the output voltage is stepped in smaller increments compared to the conventional two-level inverters. This allows harmonics mitigation at low switching frequency thereby reducing switching losses [13]. In addition, the low dv/dt of the MLI leads to a reduction of the noise generated from the switching action compared to the conventional two-level inverters.

This paper proposes an energy optimized controller which is capable of compensating voltage quality disturbances. Unlike the control strategy presented in [14,15], the proposed controller maintains a balanced load-side voltage in the case of unbalanced deep

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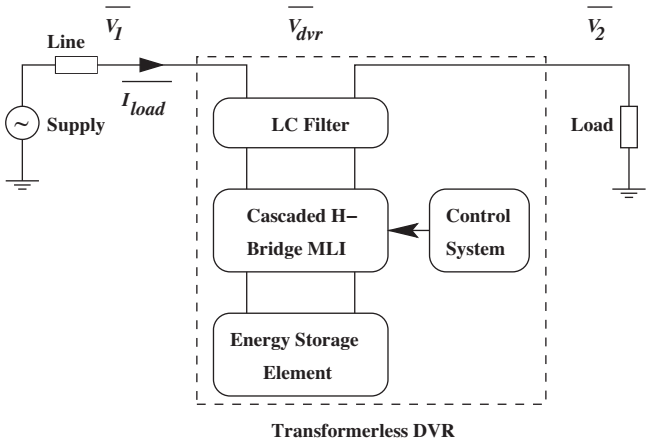

Fig. 1. Main components of the proposed DVR.

voltage sag with a reduced active power injection. The proposed scheme is characterized by an energy optimized performance which maximizes the ride-though capability of the DVR and prevents the rise in the dc-side voltage of the inverter which occurs when the DVR absorbs active power during swell compensation. This is verified by installing capacitors instead of dc sources as energy storage elements for the DVR. Furthermore, a simple and straightforward method for generating the modulation signals is utilized, which improves the DVR dynamic performance. This is in contrast to the earlier techniques in [10,14] which are based on calculating the magnitudes and the phase angles of the three-phase injected voltages of the DVR.

2. The proposed DVR system

The proposed DVR system is presented in Fig. 1. The DVR injects an appropriate voltage phasor $\bar{V}_{\text{dvr}}$ in series with the source-side voltage phasor $\bar{V}_1$ through a filter. This injected voltage keeps the load-side voltage phasor $\bar{V}_2$ undisturbed regardless of the source-side conditions.

The proposed DVR system consists of cascaded H-bridge multilevel inverter topology. Fig. 2 shows a single-phase structure of a 9-level cascaded H-bridge MLI. Many multi carrier pulse width modulation (MCPWM) switching techniques are used for the multilevel inverters such as alternative phase opposition disposition (APOD), phase opposition disposition (POD), and phase disposition (PD) [16]. The phase shifted carrier PWM (PSCPWM) is the most suitable modulation strategy for the cascaded MLI [17]. In this modulation technique, the sinusoidal reference waveforms for the two legs of each H-bridge inverter are phase shifted by 180°, while the carriers of the H-bridge inverters are phase shifted by $180^\circ/N$ (where N is the number of the H-bridge inverters in a phase leg of the MLI). It is noteworthy that applying the PSCPWM switching technique ensures equal loading between the batteries in each phase of the cascaded H-bridge MLI. Moreover, this strategy leads to a significant reduction of the harmonic content of the MLI [16]. Fig. 3 illustrates the carriers and modulating signals for a single-phase, 9-level, cascaded MLI with the modulation frequency of 50 Hz and the carrier frequency of 750 Hz (frequency ratio $m_f = 15$).

3. The proposed compensation scheme

With the DVR installed in the system and assuming a balanced linear load, both load-side voltage and load current are balanced even if the source-side voltage is distorted or unbalanced. Then

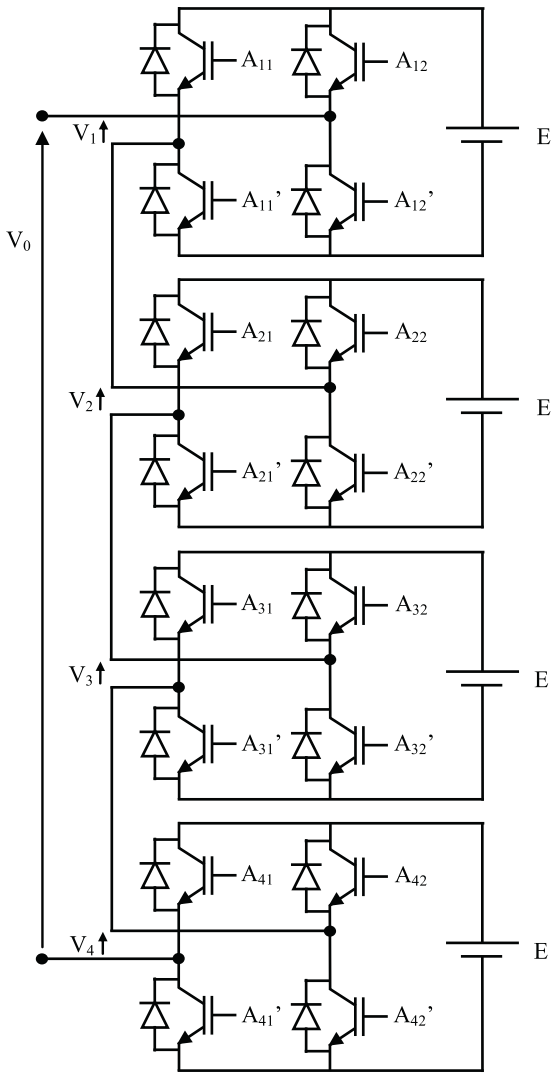

Fig. 2. Single-phase 9-level cascaded H-bridge MLI.

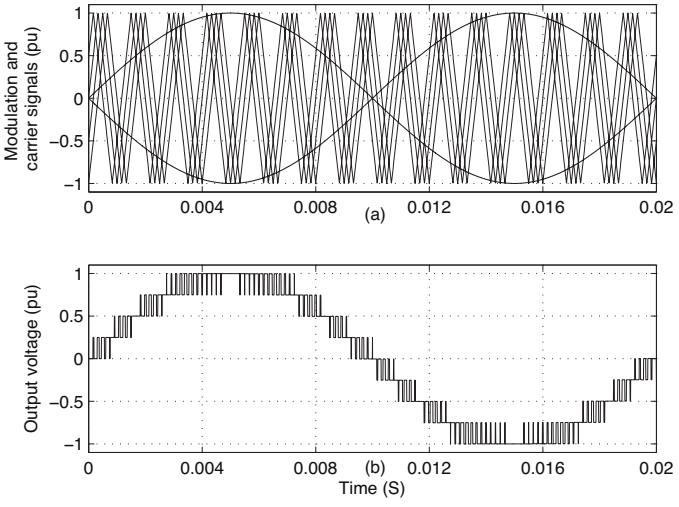

Fig. 3. The PSCPWM technique for a 9-level cascaded H-bridge MLI.

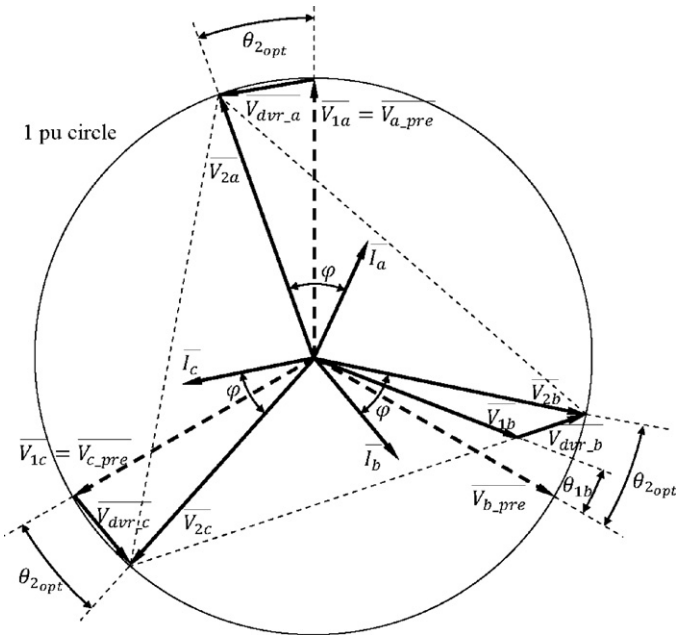

Fig. 4. Three-phase phasor diagram of restoring the load-side voltage using the proposed compensation technique.

the active power of load-side, P_{load}, and source-side, P_{source}, can be given by:

$$P_{\text{load}} = 3V_2 I\cos\varphi, \tag{1}$$

and

$$P_{\text{source}} = I[V_{1a}\cos(\varphi-\theta_{2\,\text{opt}}+\theta_{1a}) + V_{1b}\cos(\varphi-\theta_{2\,\text{opt}}+\theta_{1b}) + V_{1c}\cos(\varphi-\theta_{2\,\text{opt}}+\theta_{1c})], \tag{2}$$

where I is the load current; V_{1a}, V_{1b}, and V_{1c} are the source-side voltage magnitudes; $\theta_{2\,\text{opt}}$ is the phase angle of the load-side voltage with respect to the pre-sag voltage; θ_{1a}, θ_{1b}, and θ_{1c} are the phase angles of the source-side voltage with respect to the pre-sag voltage; φ is the load power factor angle.

The active power injected by the DVR into the system, P_{dvr}, can be expressed as:

$$P_{\text{dvr}} = P_{\text{load}} - P_{\text{source}} = 3V_2 I\cos\varphi - I[V_{1a}\cos(\varphi-\theta_{2\,\text{opt}}+\theta_{1a}) + V_{1b}\cos(\varphi-\theta_{2\,\text{opt}}+\theta_{1b}) + V_{1c}\cos(\varphi-\theta_{2\,\text{opt}}+\theta_{1c})] \tag{3}$$

The main concept of the proposed compensation strategy is that the DVR active power depends on the angle $\theta_{2\,\text{opt}}$. The three-phase voltages at the load-side can be restored to 1 pu with a new phase angle $\theta_{2\,\text{opt}}$ that optimizes the active power of the DVR. This angle should guarantee that the load-side voltage remains balanced during compensation. Fig. 4 portrays the three-phase phasor diagram of restoring the load-side voltage in case of a single-phase sag in phase '*b*' (the three-phase load-side voltages $\bar{V}_{2a}$, $\bar{V}_{2b}$, and $\bar{V}_{2c}$ are balanced).

3.1. Zero active power mode

The DVR can operate with zero active power by injecting V_{dvr} in a way such that V_2 is restored to 1 pu with an angle of $\theta_{2\,\text{opt}} = \theta_{2\,\text{zero}}$, where $\theta_{2\,\text{zero}}$ is the phase angle of the load-side voltage with respect to the pre-sag voltage required to achieve compensation with $P_{\text{dvr}} = 0$.

Taking the pre-fault voltages ($\bar{V}_{\text{pre\_}a}$, $\bar{V}_{\text{pre\_}b}$, and $\bar{V}_{\text{pre\_}c}$) as references for their phases, the angle $\theta_{2\,\text{zero}}$ can be calculated by substituting $P_{\text{dvr}} = 0$ in (3), which results in

$$3V_2 I\cos\varphi = I[V_{1a}\cos(\varphi-\theta_{2\,\text{zero}}+\theta_{1a}) + V_{1b}\cos(\varphi-\theta_{2\,\text{zero}}+\theta_{1b}) + V_{1c}\cos(\varphi-\theta_{2\,\text{zero}}+\theta_{1c})] \tag{4}$$

Simplifying (4) to

$$\begin{aligned}3V_2\cos\varphi = {} & V_{1a}[\cos(\varphi-\theta_{2\,\text{zero}})\cos\theta_{1a} - \sin(\varphi-\theta_{2\,\text{zero}})\sin\theta_{1a}] \\ & + V_{1b}[\cos(\varphi-\theta_{2\,\text{zero}})\cos\theta_{1b} - \sin(\varphi-\theta_{2\,\text{zero}})\sin\theta_{1b}] \\ & + V_{1c}[\cos(\varphi-\theta_{2\,\text{zero}})\cos\theta_{1c} - \sin(\varphi-\theta_{2\,\text{zero}})\sin\theta_{1c}]\end{aligned} \tag{5}$$

Eq. (5) can be written in the form

$$3V_2\cos\varphi = A\cos(\varphi-\theta_{2\,\text{zero}}) - B\sin(\varphi-\theta_{2\,\text{zero}}) \tag{6}$$

where

$$A = V_{1a}\cos\theta_{1a} + V_{1b}\cos\theta_{1b} + V_{1c}\cos\theta_{1c} \tag{7}$$

$$B = V_{1a}\sin\theta_{1a} + V_{1b}\sin\theta_{1b} + V_{1c}\sin\theta_{1c} \tag{8}$$

Consider A and B are two sides at right-angle of a triangle, they can be written as follows:

$$A = \sqrt{A^2+B^2}\cos\beta \tag{9}$$

$$B = \sqrt{A^2+B^2}\sin\beta \tag{10}$$

where

$$\beta = \tan^{-1}\left(\frac{B}{A}\right) \tag{11}$$

By substituting (9)–(11) in (6)

$$3V_2\cos\varphi = \sqrt{A^2+B^2}\cos(\varphi-\theta_{2\,\text{zero}}+\beta) \tag{12}$$

Assuming the load-side voltage V_2 is restored at 1 pu, the phase angle of the load-side voltage that result in zero active power is

$$\theta_{2\,\text{zero}} = \varphi + \beta - \cos^{-1}\frac{3\cos\varphi}{\sqrt{A^2+B^2}}. \tag{13}$$

Eq. (13) leads to the following condition:

$$\lambda = \frac{3\cos\varphi}{\sqrt{A^2+B^2}} \le 1 \tag{14}$$

If (14) is satisfied, the voltage disturbance can be compensated with zero active power injection and the compensation is achieved with only reactive power injection.

3.2. Minimum active power mode

If (14) is not satisfied, the compensation cannot be done with zero active power injection. In this case, the DVR can be controlled to operate in the minimum active power mode. The load-side voltage is restored to 1 pu with a phase angle $\theta_{2\,\text{opt}} = \theta_{2\,\text{min}}$, where $\theta_{2\,\text{min}}$ is the calculated phase angle of the load-side voltage with respect to the pre-sag voltage to minimize the power injection from the DVR during compensation. To find the angle $\theta_{2\,\text{min}}$, differentiate (3) as follows:

$$\frac{\partial P_{\text{dvr}}}{\partial\theta_{2\,\text{min}}} = 0 = -I[V_{1a}\sin(\varphi-\theta_{2\,\text{min}}+\theta_{1a}) + V_{1b}\sin(\varphi-\theta_{2\,\text{min}}+\theta_{1b}) + V_{1c}\sin(\varphi-\theta_{2\,\text{min}}+\theta_{1c})] \tag{15}$$

Expanding (15)

$$V_{1a}[\sin(\varphi-\theta_{2\min})\cos\theta_{1a}+\cos(\varphi-\theta_{2\min})\sin\theta_{1a}] +V_{1b}[\sin(\varphi-\theta_{2\min})\cos\theta_{1b}+\cos(\varphi-\theta_{2\min})\sin\theta_{1b}] +V_{1c}[\sin(\varphi-\theta_{2\min})\cos\theta_{1c}+\cos(\varphi-\theta_{2\min})\sin\theta_{1c}]=0 \quad (16)$$

Using (7) and (8), (16) can be written as

$$\tan(\varphi-\theta_{2\min})=-\frac{B}{A} \quad (17)$$

Using (11), $\theta_{2\min}$ can be written as

$$\theta_{2\min}=\varphi+\beta \quad (18)$$

To check that this value of $\theta_{2\min}$ minimize the active power injection of the DVR, the value of $\partial^2 P_{\text{dvr}}/\partial\theta^2_{2\min}$ must be positive at $\theta_{2\min}=\varphi+\beta$.

$$\frac{\partial^2 P_{\text{dvr}}}{\partial\theta^2_{2\min}}=I[V_{1a}\cos(\varphi-\theta_{2\min}+\theta_{1a})+V_{1b}\cos(\varphi-\theta_{2\min}+\theta_{1b}) +V_{1c}\cos(\varphi-\theta_{2\min}+\theta_{1c})] \quad (19)$$

Substituting $\theta_{2\min}=\varphi+\beta$

$$\frac{\partial^2 P_{\text{dvr}}}{\partial\theta^2_{2\min}}=I[V_{1a}\cos(\theta_{1a}-\beta)+V_{1b}\cos(\theta_{1b}-\beta) +V_{1c}\cos(\theta_{1c}-\beta)] \quad (20)$$

Expanding (20)

$$\frac{\partial^2 P_{\text{dvr}}}{\partial\theta^2_{2\min}}=I[V_{1a}(\cos\theta_{1a}\cos\beta+\sin\theta_{1a}\sin\beta) +V_{1b}(\cos\theta_{1b}\cos\beta+\sin\theta_{1b}\sin\beta) +V_{1c}(\cos\theta_{1c}\cos\beta+\sin\theta_{1c}\sin\beta)] \quad (21)$$

Using (7) and (8), (21) can be written as

$$\frac{\partial^2 P_{\text{dvr}}}{\partial\theta^2_{2\min}}=I(A\cos\beta+B\sin\beta)=I\sqrt{A^2+B^2} \quad (22)$$

Since the value of the square root $\sqrt{A^2+B^2}$ is always positive, the DVR power is minimum at $\theta_{2\min}=\varphi+\beta$ and its value is:

$$P_{\text{dvr\_min}}=I[3V_2\cos\varphi-V_{1a}\cos(\theta_{1a}-\beta)-V_{1b}\cos(\theta_{1b}-\beta) -V_{1c}\cos(\theta_{1c}-\beta)] \quad (23)$$

4. Generation of the modulation signals

Generation of the modulation signals for the three phases of the DVR MLI must be done without delay to avoid affecting the performance of the DVR. This can be achieved by generating three reference waveforms ($\bar{V}_{2a\_star}$, $\bar{V}_{2b\_star}$, and $\bar{V}_{2c\_star}$) which represent the required load-side three-phase voltages. These signals are generated with 50 Hz frequency, 1 pu magnitude, and phase angle $\theta_{2\,\text{opt}}$, such that

$$\begin{aligned}\bar{V}_{2a\_star}&=1\angle\theta_{2\,\text{opt}}\\ \bar{V}_{2b\_star}&=1\angle(\theta_{2\,\text{opt}}-120^\circ)\\ \bar{V}_{2c\_star}&=1\angle(\theta_{2\,\text{opt}}+120^\circ)\end{aligned} \quad (24)$$

The required modulation signals of the three-phase DVR voltages can be calculated by subtracting the uncompensated source-side three-phase voltages from the generated reference waveforms as follows:

$$\begin{aligned}\bar{V}_{\text{mod\_}a}&=\bar{V}_{2a\_\text{star}}-\bar{V}_{1a}\\ \bar{V}_{\text{mod\_}b}&=\bar{V}_{2b\_\text{star}}-\bar{V}_{1b}\\ \bar{V}_{\text{mod\_}c}&=\bar{V}_{2c\_\text{star}}-\bar{V}_{1c}\end{aligned} \quad (25)$$

This is a simple and straightforward method for generating the modulation signals, which improves the DVR dynamic performance compared to the techniques used in [10,14] which are based on calculating the magnitudes and the phase angles of the three-phase injected voltages of the DVR. The block diagram of the proposed compensation algorithm is shown in Fig. 5.

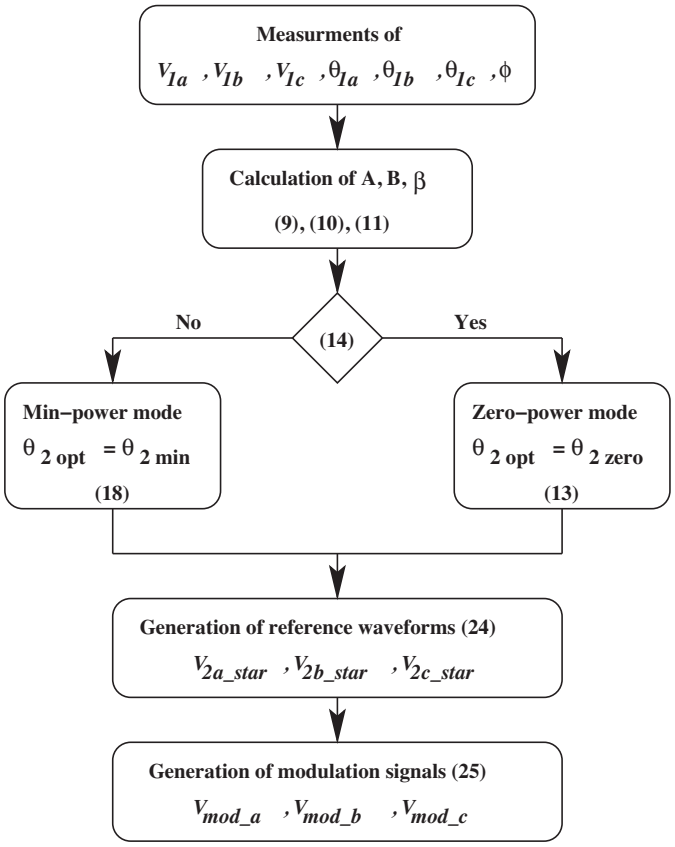

Fig. 5. Block diagram of the proposed compensation algorithm. *Note*: Parenthetical numbers refer to equation numbers in the text.

5. Simulation results

The performance of the proposed DVR system is tested by considering different cases of voltage disturbances such as balanced and unbalanced sags, swells, flicker, and long duration voltage variation. A simple distribution system, shown in Fig. 1, is implemented in the PSCAD/EMTDC simulation package to assess the dynamic performance of the proposed compensation scheme. It consists of a three-phase 11 kV, 50 Hz source, and a feeder that delivers power to a load of 1.4 MW and 80.92% lagging power factor. The separate dc sources of the 9-level inverter of the transformerless DVR are 2 kV each. A simple LC filter with C_f = 0.5 mH and L_f = 300 μF is used to eliminate the switching frequency harmonics from the output voltage of the inverter.

5.1. Voltage sag mitigation

The DVR is turned-on at t = 0.05 s, where the source-side voltage is 0.988 pu. At t = 0.1 s, the supply-side is subjected to a

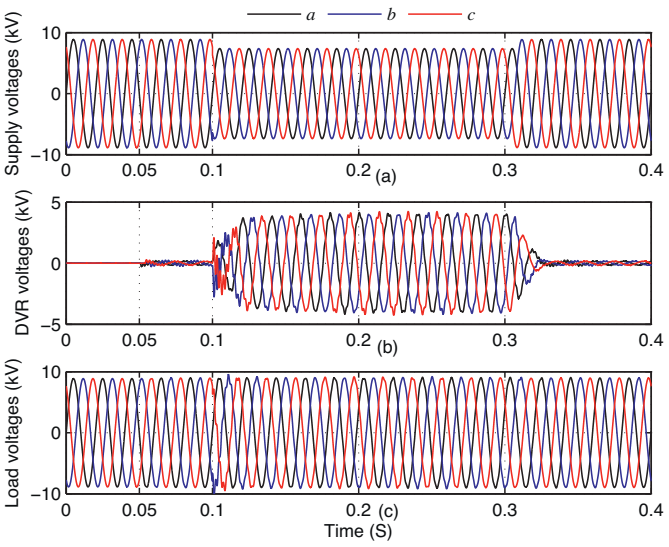

Fig. 6. Three-phase waveforms during a shallow three-phase balanced voltage sag to 82.1%: (a) source-side voltage, (b) injected voltage, and (c) load-side voltage.

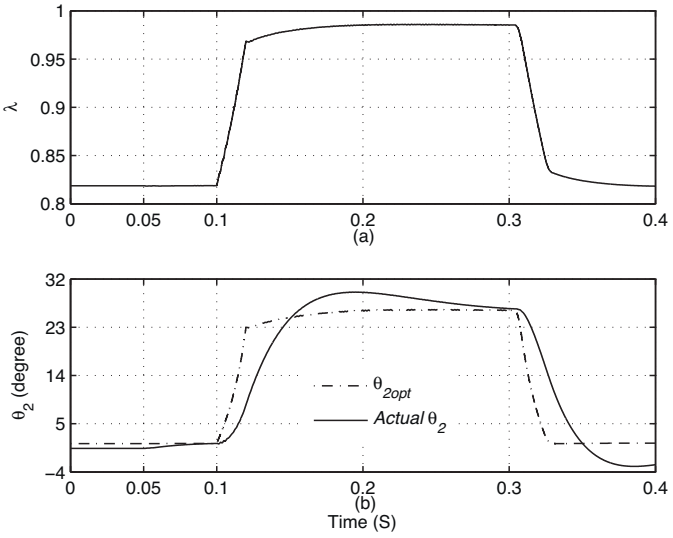

Fig. 8. Parameters of the proposed control algorithm: (a) the factor λ and (b) the actual and optimal values of the phase angle of the load-side voltage.

three-phase balanced fault that cause a shallow voltage sag to 82.1% for 10 cycles. Fig. 6 shows the three-phase waveforms of the supply-side voltages, the injected voltages by the DVR, and the restored load-side voltages. The pu values of the supply-side and load-side voltages are depicted in Fig. 7(a). It is obvious that the load-side voltage is effectively regulated to its nominal value. When the fault occurs, the load voltage is recovered to 1 pu even during the transition states at the beginning and ending instants of the sag. These results reflect the accurate performance of the proposed compensation algorithm even in the transient periods. Moreover, fast load voltage recovery without overshoot is obvious from this result. After clearing the fault, the DVR works as a voltage regulator. Fig. 7(b) and (c) portrays the instantaneous active and reactive powers of the DVR, respectively. It is noteworthy that the DVR operates in the zero active power mode. This is done on the account of the reactive power generated by the DVR which is raised to 780 kVAR during the sag mitigation.

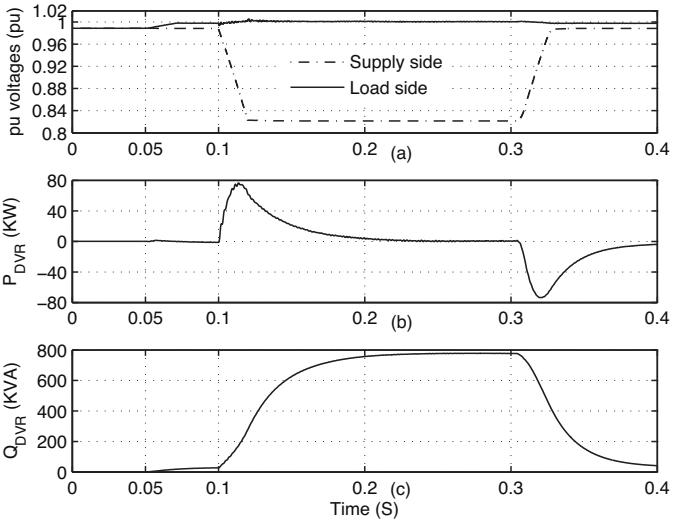

Fig. 7. Performance of the DVR during a shallow three-phase balanced voltage sag to 82.1%: (a) the pu value of supply-side and load-side voltages, (b) active power output from the DVR, and (c) reactive power output from the DVR.

Fig. 8(a) traces the factor λ which is less than 1 before and after the sag incident. Recall that when the factor λ, as calculated in Eq. (14), has a value less than one, that means that the disturbance can be compensated by injecting only reactive power, not real power as indicated in Fig. 7(b). This action means that the injected voltage and the load current are orthogonal. Fig. 9 examines this fact during and after the sag incident. The measured (actual) phase-angle of the load-side voltage, θ_2, and its optimal value, $\theta_{2\,\mathrm{opt}}$, estimated from (13) are traced in Fig. 8(b). Once the DVR is switched on at $t = 0.05$, θ_2 successfully tracks $\theta_{2\,\mathrm{opt}}$. It should be noted that $\theta_{2\,\mathrm{opt}}$ is increased during the fault period to allow for increasing the reactive power injected by the DVR, as indicated in Fig. 7(c), to compensate the sag with zero active power.

The DVR operates in the minimum active power mode to compensate for deep voltage sag. Fig. 10 portrays the three-phase waveforms of the supply-side voltages, the injected voltages, and the load-side voltages when the system is subjected to a three-phase balanced deep sag to 66%. The supply-side voltage drops to 0.66 pu while the load-side voltage is recovered to 1 pu as indicated in Fig. 11(a). The DVR operates in the minimum active power mode

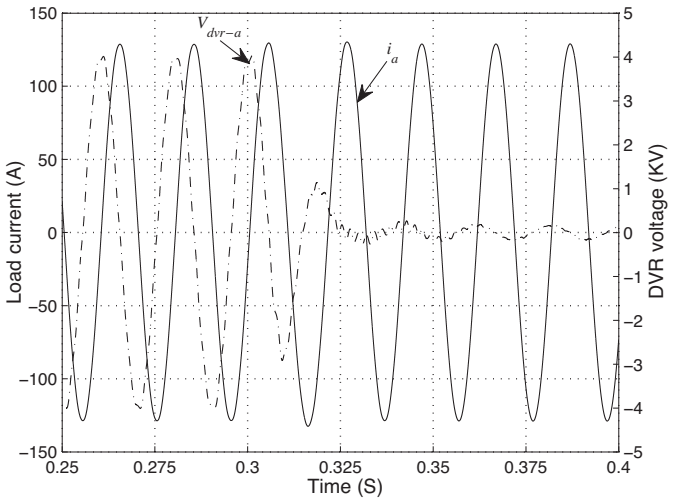

Fig. 9. Phase *a* load current and the injected voltage by the DVR.

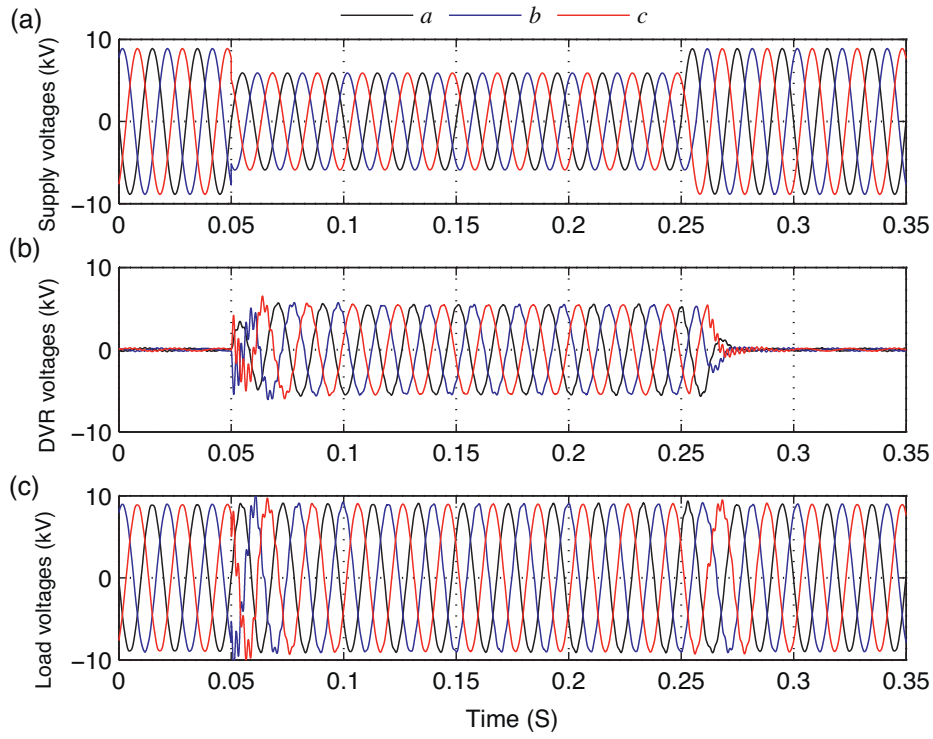

Fig. 10. Three-phase waveforms during a deep three-phase balanced voltage sag to 66%: (a) the source-side voltage, (b) the injected voltage, and (c) the load-side voltage.

with P_{dvr} = 275 kW and Q_{dvr} = 1020 kVAR as shown in Fig. 11(b) and (c), respectively.

Finally, the system is subjected to unbalanced voltage sag in phase '*a*' to 49.6%. Fig. 12 demonstrates that the DVR injects voltage in the three phases (not only in phase '*a*') to balance as well as to compensate the load-side voltage at unity as shown in Fig. 13(a). Fig. 13(b) illustrates that the compensation is done with the DVR operating in the zero active power mode as (14) is satisfied.

It is obvious that the proposed control algorithm succeeds in compensating for the voltage sag/unbalance, and tightly regulating the phase voltage to the nominal value during the fault period

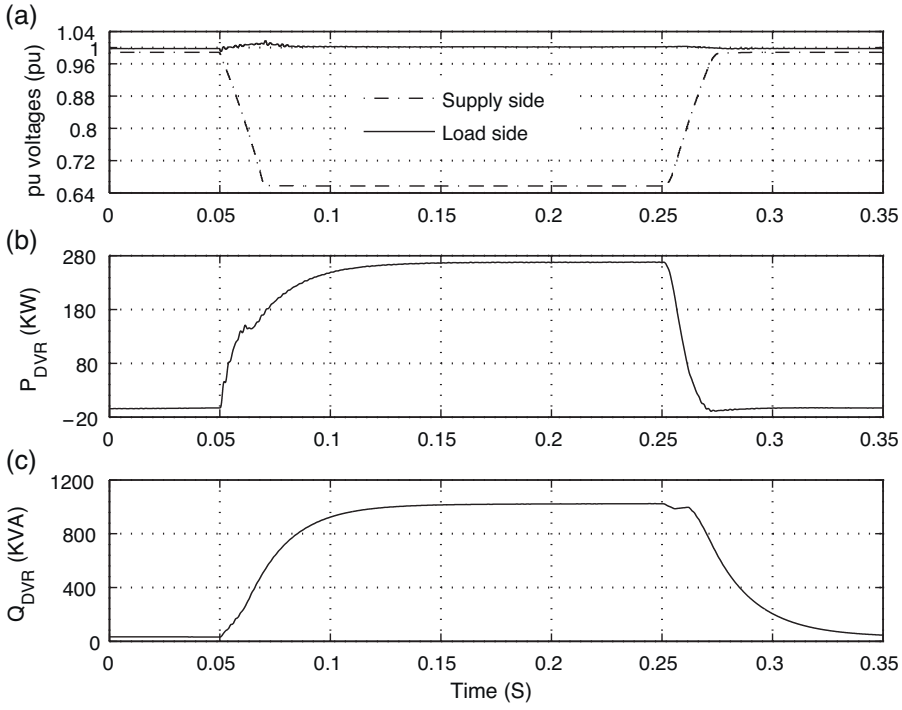

Fig. 11. Performance of the DVR during a deep three-phase balanced voltage sag to 66%: (a) the pu value of the supply-side and load-side voltages, (b) active power output from the DVR, and (c) reactive power output from the DVR.

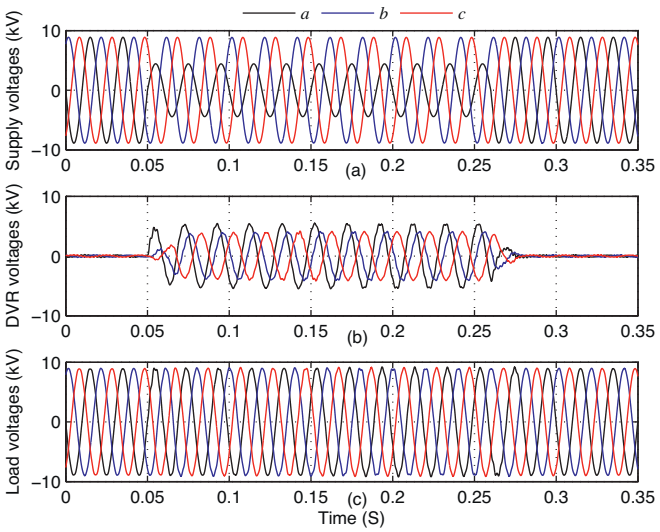

Fig. 12. Three-phase waveforms during single-phase voltage sag to 49.6% in phase '*a*': (a) the source-side voltage, (b) the injected voltage, and (c) the load-side voltage.

with a fast response. These results validate the robustness of the proposed DVR system.

For balanced sag compensation, the active power injected by the DVR using either the proposed scheme or the technique presented in [15] is the same. Fig. 14 plots the active power injected by the DVR against single-phase voltage sag for the proposed compensation scheme and the technique presented in [15]. Both traces are obtained for the system under study with the same load power factor. Using the proposed compensation technique, the DVR restores the load-side voltage without supplying any active power up to 0.575 pu voltage sag. If the sag is deeper than 0.575 pu, the DVR needs to supply less active power than that supplied by the compensation technique of [15]. It is evident that the proposed compensation scheme extends the limit of the DVR to operate in the zero active power mode compared to the technique of [15] which causes the DVR to inject active power to compensate for sags deeper than 0.19 pu. In turn, the energy saving and the ride-through capability the DVR using the proposed compensation technique are significantly enhanced.

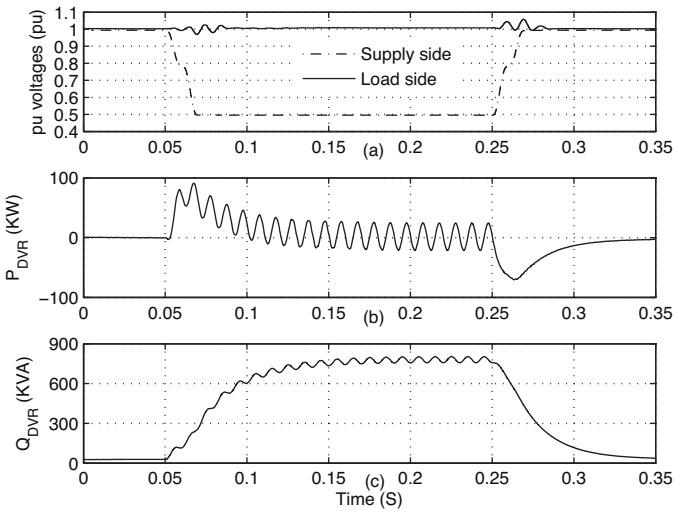

Fig. 13. Performance of the DVR during single-phase voltage sag to 49.6% in phase '*a*': (a) the pu value of the supply-side and load-side voltages, (b) active power output from the DVR, and (c) reactive power output from the DVR.

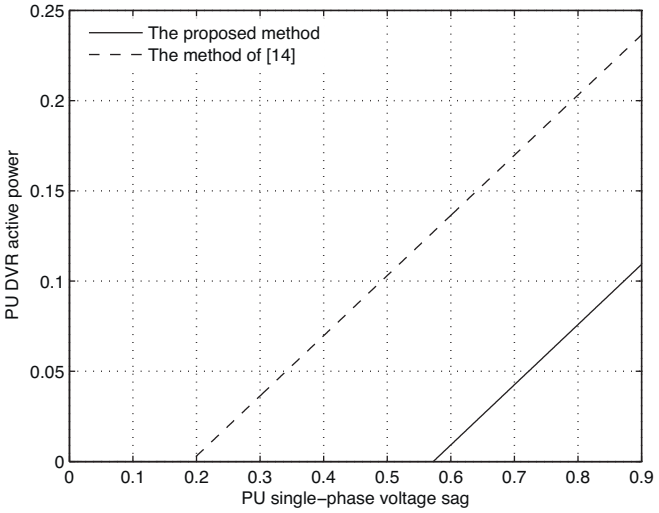

Fig. 14. Active power injected by the DVR versus single-phase voltage sag.

5.2. Voltage swell mitigation

The condition of (14) is always satisfied for voltage swells, which guarantees that no active power is absorbed by the DVR during the swell compensation. In turn, there will be no rise in the dc-link voltage if the batteries are replaced by capacitors.

Fig. 15 depicts the three-phase waveforms of the source-side voltages, the injected voltages, and the load-side voltages during a voltage swell to 119%. Fig. 16(a) portrays the supply-side and the load-side voltage which is successfully restored to 1 pu. The swell compensation is achieved without drawing active power from the DVR, while it absorbs reactive power of 500 kVAR as demonstrated in Fig. 16(b) and (c), respectively.

5.3. Flicker suppression

In this case, the system is subjected to an unbalanced voltage flicker (single-phase voltage flicker in phase '*a*') during the first 250 ms. At $t = 0.26$ s, a balanced three-phase voltage flicker is

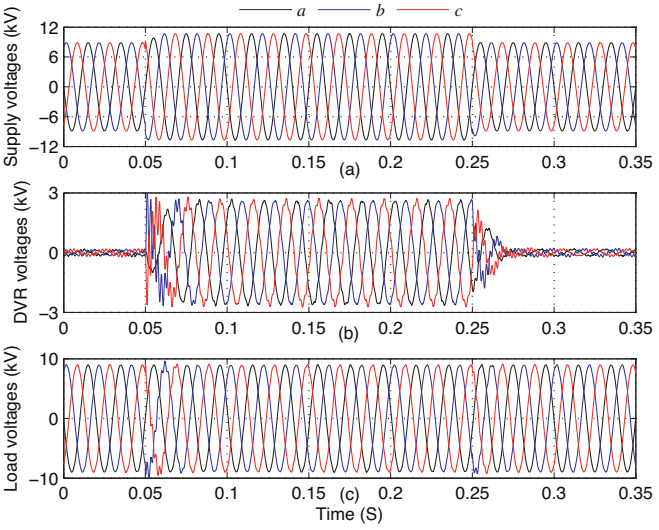

Fig. 15. Three-phase waveforms during three-phase balanced voltage swell to 119%: (a) the source-side voltage, (b) the injected voltage, and (c) the load-side voltage.

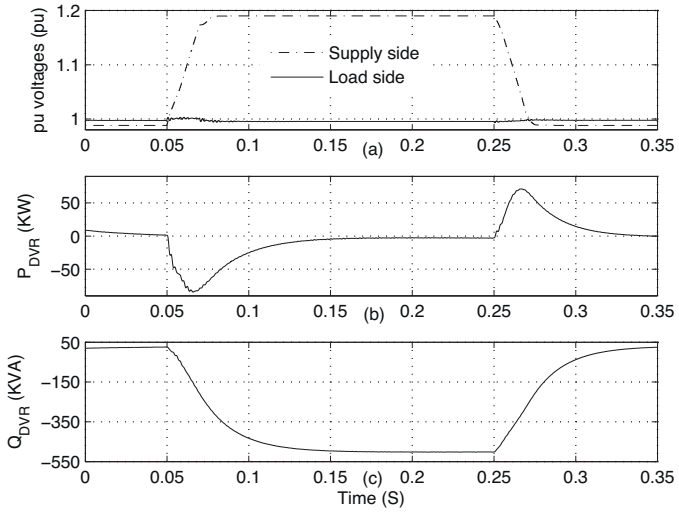

Fig. 16. Performance of the DVR during three-phase balanced voltage swell to 119%: (a) the pu value of the supply-side and load-side voltages, (b) active power output from the DVR, and (c) reactive power output from the DVR.

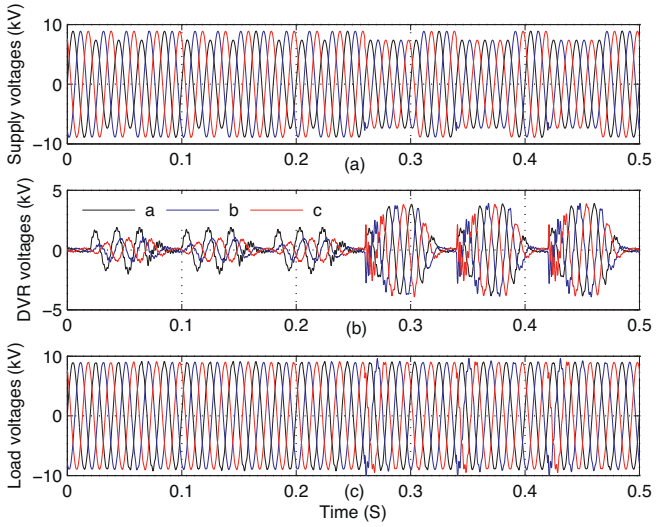

Fig. 17. Three-phase waveforms during single and three-phase voltage flicker: (a) the source-side voltage, (b) the injected voltage, and (c) the load-side voltage.

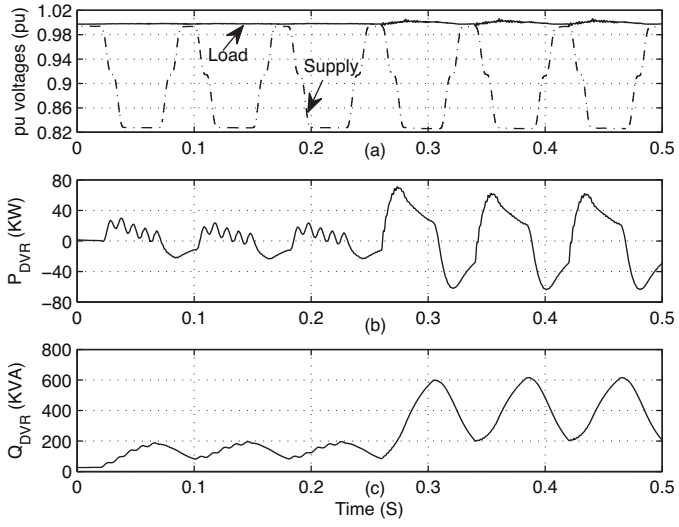

Fig. 18. Performance of the DVR during single and three-phase voltage flicker: (a) the pu value of the supply-side and load-side voltages, (b) active power output from the DVR, and (c) reactive power output from the DVR.

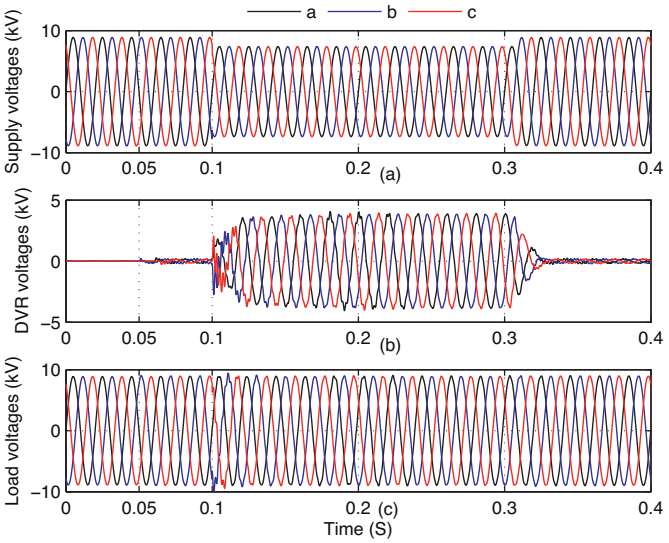

Fig. 19. Three-phase waveforms when the batteries are replaced by capacitors: (a) the source-side voltage, (b) the injected voltage, and (c) the load-side voltage.

initiated. The voltage flicker has an amplitude of 0.172 pu and a frequency of 12.5 Hz.

Fig. 17 displays the waveforms of the supply-side voltages, the injected voltages, and the load-side voltages. The voltage flicker is effectively compensated as indicated in Figs. 17(c) and 18(a). Fig. 18(b) and (c) portrays the instantaneous active power and reactive power of the DVR. The compensation is done with zero average active power as can be shown in Fig. 18(b). As expected, the reactive power supplied from the DVR increases in the case of the three-phase flicker and it is oscillating with the frequency of the flicker waveform.

5.4. Operating the proposed DVR system using capacitors

One of the main advantages of the proposed compensation scheme is the capability of replacing the dc power supplies, at the dc-side of the inverter, by capacitors as energy storage elements. This action reduces the cost and the weight of the DVR. This study case is dedicated to examine the ability of the proposed

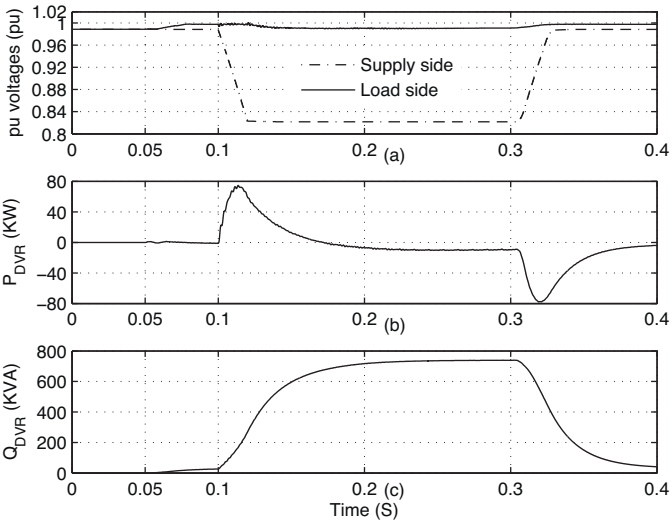

Fig. 20. Performance of the DVR when the batteries are replaced by capacitors: (a) the pu value of the supply-side and load-side voltages, (b) active power output from the DVR, and (c) reactive power output from the DVR.

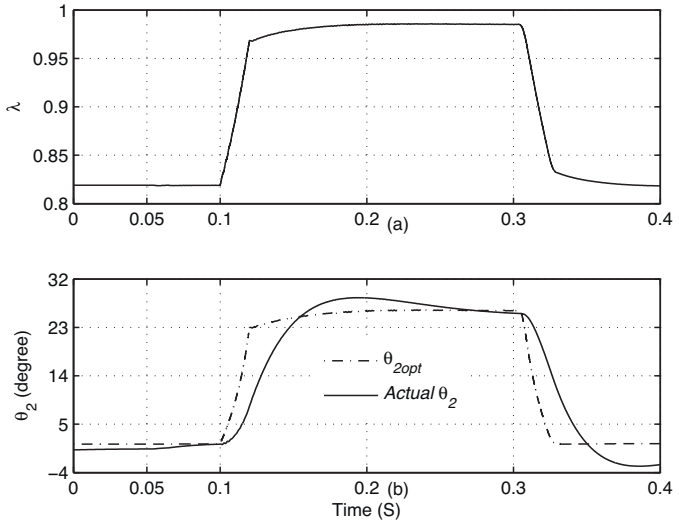

Fig. 21. Parameters of the proposed control algorithm when the batteries are replaced by capacitors: (a) the factor λ and (b) the actual and optimal values of the phase angle of the load-side voltage.

compensation control system to maintain the dc voltage level of the capacitors, while mitigating a three-phase voltage sag to 82.1% similar to the first case study. The installed capacitors are 3000 μF, 2 kV, at each dc-side of the single-phase inverters of the cascaded MLI.

As shown in Figs. 19 and 20(a), the load voltage is effectively recovered to 0.99 pu. Since the factor λ, traced in Fig. 21(a), is less than 1, the DVR compensates the sag with zero active power as indicated in Fig. 20(b). During the sag compensation, the DVR absorbs a small quantity of active power to sustain the dc-side voltages of the cascaded MLI. The actual phase-angle of the load-side voltage and its optimal value are portrayed in Fig. 21(b). The results are very close to that of the first case study.

The capacitor voltages are changing by small percentage during the compensation as displayed in Fig. 22 due to zero active power injection from the DVR. In addition, the PSCPWM switching technique keeps the equal loading condition between the H-bridges in each phase of the cascaded MLI. In turn, the capacitor voltages are nearly balanced. If the proposed DVR is required to mitigate long-duration voltage disturbances, a dc-side voltage regulation loop should be added to the proposed control system.

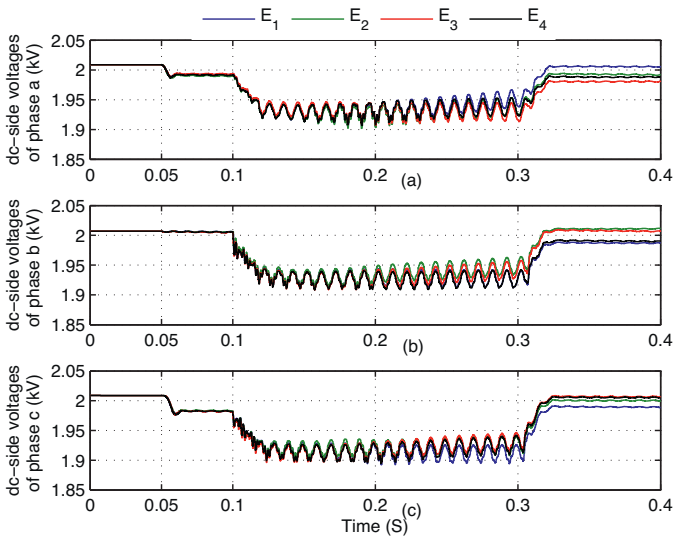

Fig. 22. Capacitor voltages of the H-bridges used in the proposed DVR system.

6. Conclusions

This paper presents an energy optimized scheme for the DVR to compensate for different voltage quality disturbances. A transformerless DVR based on cascaded H-bridge MLI, which is suitable for medium voltage distribution networks, is utilized. The elimination of the insertion transformer provides effective reduction of both cost and size of the DVR. The proposed compensation scheme controls the phase angle of the load-side voltage to optimize the active power of the DVR while compensating the load-side voltage at unity. Depending on the supply-side voltage phasor, the DVR can operate in either zero or minimum active power mode. A simple technique of generating the modulation signals is utilized to compensate the load-side voltage even during the transition periods of the disturbance. A superior advantage of the proposed control method is the maximization of the ride-through capabilities of the DVR during sag compensation. In turn, capacitors can be used to replace the power source from the dc-side of the DVR. Different simulation study cases are demonstrated to assess the potential application of the proposed control approach. A fast response and accurate compensation with optimum energy of the proposed control system are revealed in the simulation results.

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