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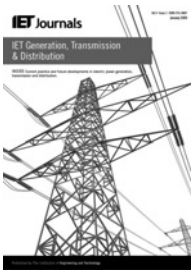

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Design and analysis of dynamic voltage restorer for deep voltage sag and harmonic compensation

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Abstract: A dynamic voltage restorer (DVR) to compensate deep voltage sags and harmonics is proposed. The DVR consists of shunt and series converters connected back-to-back through a dc-to-dc step up converter. The presence of the dc-to-dc step converter permits the DVR to compensate deep voltage sags for long duration. The series converter is connected to the supply side whereas the shunt converter is connected to the load side. With this configuration, there is no need for large dc capacitors. A design procedure for the components of the DVR is presented under a voltage sag condition. The control system of the proposed DVR is based on hysteresis voltage control. Besides voltage sag compensation, the capability of compensating load voltage harmonics has been added to the DVR to increase the power quality benefits to the load with almost negligible effect on the sag compensation capability. The proposed DVR is modelled and simulated using SIMULINK/MATLAB environment. Time domain simulations are used to verify the operation of the DVR with linear and non-linear loads.

1 Introduction

Dynamic voltage restorer (DVR) is a series-connected flexible ac transmission systems (FACTS) controller used to compensate voltage sags and swells during abnormal conditions in distribution systems [1, 2]. There are different system topologies of the DVR, which have been evaluated and ranked in [3]. In [3], four different system topologies for DVR have been analysed and tested with focus on the method used to acquire the necessary energy during voltage sags. Two topologies take energy from the grid and the other two topologies take energy from the energy storage devices during the voltage sag. These topologies are: (i) DVR with no storage and supply-side-connected shunt converter, (ii) DVR with no storage and load-side-connected shunt converter, (iii) DVR with energy storage with variable dc-link-voltage and (iv) DVR with energy storage and with constant-dc link voltage. Experimental and simulations have been performed to rank these topologies depending on the required performance and cost of the DVR. Overall evaluation has shown that topology number 2 has the highest score.

The performance analysis and control of the DVR, with different circuit topologies, have been studied and examined by researchers in the literature [4–10]. In [4], different control methods for the DVR have been analysed with emphasis on the compensation of voltage sag with phase jump. Two methods, which are designated as 'in-phase compensation' and 'pre-sag compensation' in [4], have been proposed and compared. Experimental results have validated the feasibility of these methods. In [5], a robust control method with an outer H_∞ voltage control loop and an inner current control loop has been designed and tested on a laboratory DVR system. Experimental tests with linear load, non-linear load and induction motor load have been performed to validate the proposed control scheme. In [6], the operating principles of the DVR compensating unbalanced and/or distorted loads have been presented. A dc capacitor supported DVR has been proposed so that no active power exchange exists in the system. This technique has been validated using extensive digital simulations. In [7], a fast dynamic control scheme for capacitor supported for a single-phase DVR has been proposed. The control scheme has two control loops; the

inner loop and the outer loop which are, respectively, responsible for generating the gate signal of the switches of the DVR and the reference voltage signal of the DVR. A DVR prototype has been built and tested with non-linear load. A novel control strategy, which has been validated using time domain simulations, for the capacitor supported DVR has been proposed in [8] to compensate voltage sags. The possibility of compensating harmonics using DVR at medium voltage level has been investigated in [9]. A control strategy has been included in the main control system of the DVR to compensate selected harmonics during steady state. The topology of the used DVR is based on a dc capacitor supported DVR.

In this paper, a DVR with the capability to compensate harmonics and deep voltage sags is proposed. The proposed DVR is a DVR with no storage and load-side-connected shunt converter to obtain the maximum benefits from the device [3]. In addition, dc-to-dc step up converter has been introduced in the circuit as shown in Fig. 1. The main function of the step up dc-to-dc converter is to maintain and control the dc voltage of the inverter during voltage sag. This configuration allows the DVR to compensate deep and long duration voltage sags and swells. The capability of compensating harmonics, without affecting sag or swell compensation capability, is added to the controls of the DVR. Extensive time domain simulations, with linear and non-linear loads, have been performed to validate the operation of the proposed DVR system. Digital simulation results have been shown to provide accurate predication of the behaviour of voltage-sourced converter (VSC) based FACTS devices [11].

2 Configuration and control of the DVR

The configuration of the DVR, proposed in this paper, is shown in Fig. 1. The shunt converter connected to the load side is uncontrolled rectifier, which has uncontrollable dc output voltage V_{dc1}. The uncontrolled rectifier is connected to the load bus through a step down transformer. The dc output voltage of the rectifier V_{dc1} is the input voltage of the dc-to-dc step up converter. The output voltage of the step up converter V_{dc2} is the input dc voltage of the VSC of the DVR. Although, with this configuration, the uncontrolled rectifier draws non-linear current, the DVR is able to eliminate all harmonics associated with the load voltage. In this paper, two loads are considered; $R-L$ linear load and non-linear load as shown in Fig. 2.

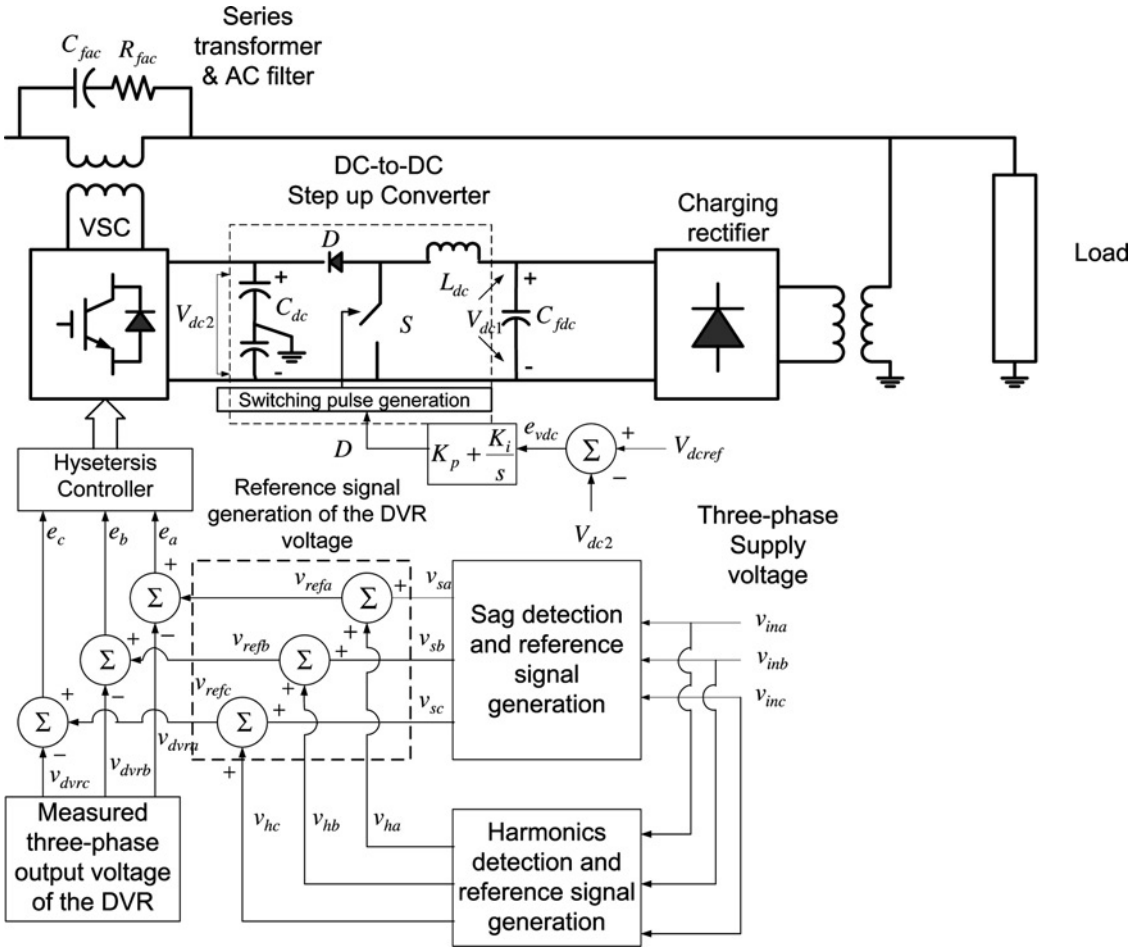

Figure 1 *Schematic diagram of the proposed DVR*

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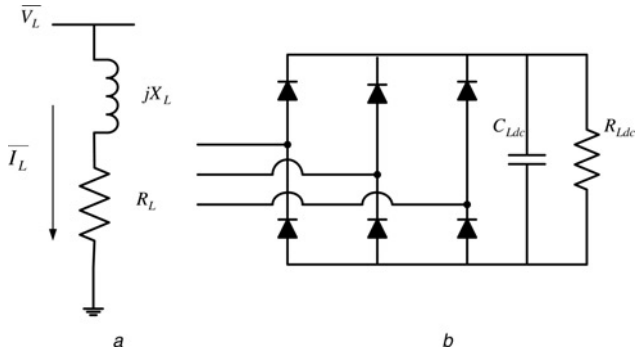

Figure 2 *Types of considered loads*

a Linear load
b Non-linear load

2.1 DC voltage control of the DVR

The step up converter controls the duty cycle D to maintain its dc output voltage V_{dc2} at the reference set value V_{dcref}. This is done using proportional and integral (PI) controller as shown in Fig. 1. The PI controller compares between V_{dcref} and V_{dc2} to produce the error e_{vdc}. The error e_{vdc} is passed through the PI controller to produce the suitable duty cycle D which in turns fed into the switching pulse generation block to generate the switching pulses of the MOSFET. In this paper, the switching frequency of the MOSFET is selected to be 20 kHz [12].

2.2 Voltage sag detection scheme

Several sag/swell detection techniques have been developed in the literature. In this paper, the sag detection method developed in [10] is used. Fig. 3 shows a SIMULINK diagram of the sag/swell detection technique. As shown in Fig. 1, the three-phase instantaneous output voltage (v_{sa}, v_{sb} and v_{sc}) from the voltage sag/swell detection block is the first reference input to the hysteresis controller block.

2.3 Harmonic's detection scheme

There are several methods to extract the harmonic components from the detected three-phase waveforms, which are instantaneous reactive power, discrete Fourier transform (DFT), recursive discrete Fourier transform (RDFT) and Kalman filtering (KF) approach [13]. In this paper, DFT approach is used, which is shown in Fig. 4. The three-phase supply distorted voltage is measured and passed to the SIMULINK block designated as discrete Fourier. In this block, the fundamental component of each phase is extracted from the corresponding distorted supply voltage. Then, the fundamental component of each phase subtracted from the corresponding distorted supply voltage to yield the harmonics presented in each phase voltage. With this arrangement, all harmonics presented in the supply voltage can be detected. The harmonics, presented in each phase, are the second reference instantaneous input voltages (v_{ha},v_{hb} and v_{hc}) to the hysteresis controller block as shown in Fig. 1.

2.4 AC voltage control of the DVR

Conventional two-level hysteresis voltage control, which is one type of non-linear voltage control based on the voltage error, is implemented. Fig. 5 shows the modelling of hysteresis voltage control using SIMULINK blocks. It consists of a comparison between the output voltage V_0 and the tolerance limits (V_H, V_L) around the reference voltage V_{ref}. Although the output voltage V_0 is between upper limit V_H and lower limit V_L, no switching occurs and when the output voltage crosses to pass the upper limit (lower band) the output voltage is decreased

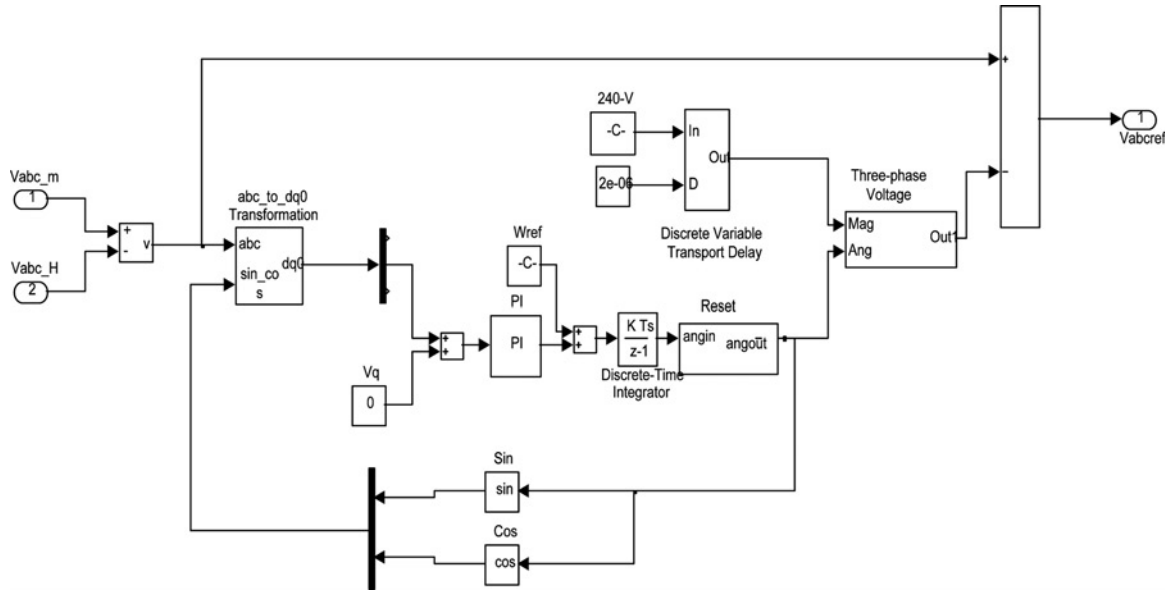

Figure 3 *SIMULINK diagram of the voltage sag detection*

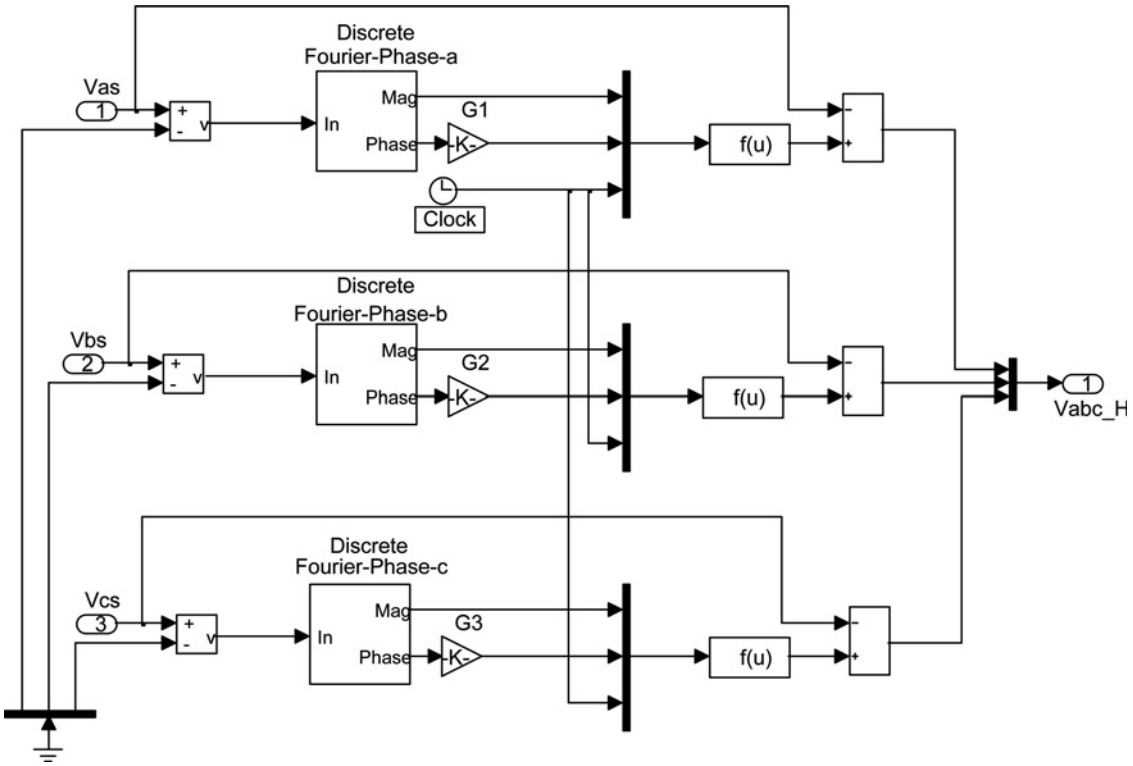

Figure 4 *SIMULINK diagram of the harmonics detection scheme*

(increased). The hysteresis band is given as $h = V_H - V_L$. In this paper, the hysteresis band is selected to be 0.000208 pu. The hysteresis controller generates the switching pulses that are fed to the VSC. The generated three-phase voltage of the DVR is injected through a series transformer. As shown in Fig. 1, an ac filters (R_{fac} and C_{fac}) are connected across the series transformer to eliminate the switching ripples produced by the VSC.

3 Design of DVR components

In this section, the dc capacitor C_{fdc} of the uncontrolled rectifier, the dc capacitor C_{dc} and the inductor L_{dc} of the dc-to-dc step up converter are designed based on single-phase voltage sag which induces a voltage fluctuation with twice the line frequency of the dc capacitor [14]. The parameters of the series and shunt transformers are the default parameters of the transformer model in SIMULINK/MATLAB. The voltage sag factor $\overline{K}_{sag}$ is defined as

$$\overline{K}_{sag} = \frac{\overline{V}_{ssag}}{\overline{V}_{spre-sag}} \tag{1}$$

where $\overline{V}_{ssag}$ is the sag load voltage and $\overline{V}_{spre-sag}$ is the pre-sag load voltage.

The magnitude of the voltage sag factor $\left|\overline{K_{sag}}\right|$ is equal to the depth of the voltage sag D_{sag}; that is

$$D_{sag} = \left|\overline{K_{sag}}\right| \tag{2}$$

The power ratings of the series PWM and the shunt uncontrolled (passive) converters in per unit of the load power are given as [3]

$$S_{shunt} = S_{series} = \frac{\left|1 - \overline{K_{sag}}\right|}{\left|\overline{K_{sag}}\right|} \tag{3}$$

where S_{shunt} is the pu power rating of the shunt converter and S_{series} is the pu power rating of the series converter.

Fig. 6 shows the relation between the total converters rating ($S_{series} + S_{shunt}$) and the voltage sag. It has to be mentioned that the DVR with load-side-connected passive converter has the highest size and superior characteristics among the other topologies [3].

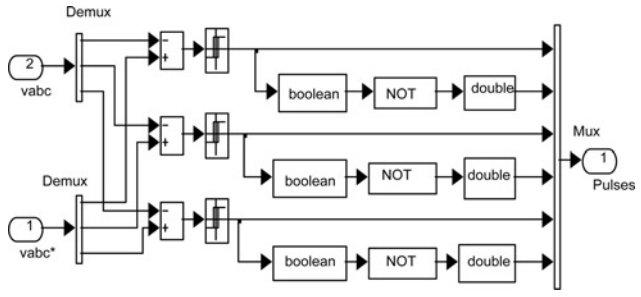

Figure 5 *SIMULINK diagram showing the hysteresis voltage controller*

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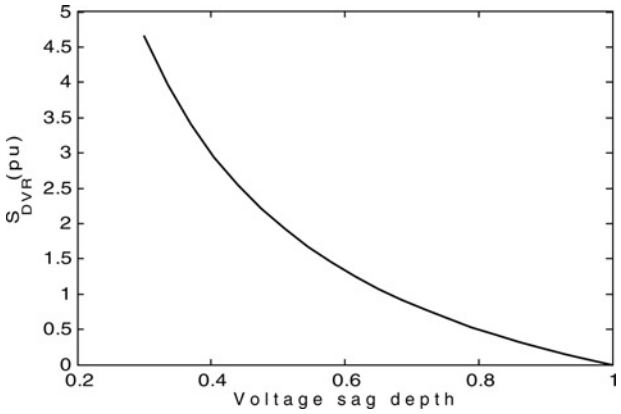

Figure 6 *Overall power rating of the DVR converters as function of the voltage sag depth (D_{sag})*

3.1 Sizing the dc capacitor C_{fdc}

The required capacitance of the dc capacitor $C_{f\mathrm{dc}}$ is given as follows [14]:

$$C_{f\,\mathrm{dc}} = \frac{D_{\mathrm{sag}} V_{\mathrm{sL-L}} I_{\mathrm{L}} \cos\Phi}{2\sqrt{3}\omega\varepsilon V_{\mathrm{dc1}}^2\left(3 - D_{\mathrm{sag}}\right)} \tag{4}$$

where $V_{\mathrm{sL-L}}$ is the line-to-line rated load voltage, I_{L} is the rated load current, $\cos\Phi$ is the power factor of the load, ω is the angular speed ($\omega = 2\pi f$), ε is the allowable dc voltage fluctuation ($\varepsilon = \Delta V_{\mathrm{dc1}}/V_{\mathrm{dc1}}$) and V_{dc1} is the dc voltage of the uncontrolled rectifier.

The dc voltage of the uncontrolled rectifier (V_{dc1}) is almost equal to the magnitude of line-to-line load voltage ($V_{\mathrm{dc1}} = V_{\mathrm{sL-L}}$) as shown in [3]. Therefore (4) can be rewritten as

$$C_{f\,\mathrm{dc}} = \frac{D_{\mathrm{sag}} I_{\mathrm{L}} \cos\Phi}{2\sqrt{3}\omega\varepsilon V_{\mathrm{sL-L}}\left(3 - D_{\mathrm{sag}}\right)} \tag{5}$$

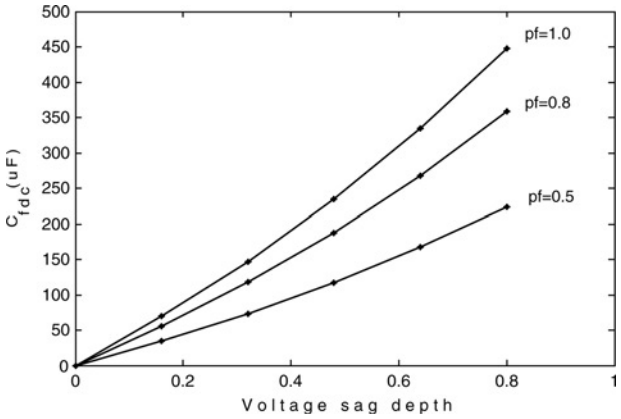

Figure 7 *Relation between dc capacitor C_{fdc} and voltage sag depth (D_{sag})*

Fig. 7 shows the relation between the size of the dc capacitor $C_{f\mathrm{dc}}$ and the voltage sag depth D_{sag} for various values of the power factor ($\cos\Phi$). In producing Fig. 7, the line-to-line voltage $V_{\mathrm{sL-L}} = 415$ V, $\omega = 2\pi f$ ($f = 50$ Hz) and $\varepsilon = 2.5\%$ are considered. It can be depicted from Fig. 7 that as voltage sag increases, the size of the dc capacitor $C_{f\mathrm{dc}}$ has to be increased because the dc capacitor should supply higher power at high sag depths. It can be seen from Fig. 7 that the loads with lower power factor allows using lower size of $C_{f\mathrm{dc}}$ since the real power, which will be supplied during the voltage sag, is lower at lower power factor. In this paper, the $C_{f\mathrm{dc}}$ is selected to be 200 μF for 0.5 voltage sag depth and 0.8 lagging power.

3.2 Sizing the inductor L_{dc} and the dc capacitor C_{dc}

The inductor L_{dc} and the capacitor C_{dc} of the dc-to-dc step up converter are given by [12]

$$L_{\mathrm{dc}} = \frac{V_{\mathrm{dc1}} D}{\Delta I_{\mathrm{dc2}} f_{\mathrm{s}}} \tag{6}$$

$$C_{\mathrm{dc}} = \frac{I_{\mathrm{dc2}} D}{\Delta V_{\mathrm{dc2}} f_{\mathrm{s}}} \tag{7}$$

where D is the duty cycle of the dc-to-dc step up converter, f_{s} is the switching frequency of the switch (MOSFET) of the dc-to-dc step up converter ($f_{\mathrm{s}} = 20$ kHz), ΔI_{dc2} is the dc output current ripple of the dc-to-dc step up converter ($\Delta I_{\mathrm{dc2}} = 0.02\%$), I_{dc2} is the dc output current of the dc-to-dc step up converter and ΔV_{dc2} is the ripple dc output voltage of the dc-to-dc step up converter ($\Delta V_{\mathrm{dc2}} = 0.02\%$).

It can be depicted from (6) that the inductor L_{dc} is directly proportional to the duty cycle D and the dc voltage of the uncontrolled converter V_{dc1}. Since $V_{\mathrm{dc1}} = V_{\mathrm{sL-L}}$ as shown in [3] and by setting $D = D_{\max}$, (6) can be rewritten as

$$L_{\mathrm{dc}} = \frac{V_{\mathrm{sL-L}} D_{\max}}{\Delta I_{\mathrm{dc2}} f_{\mathrm{s}}} \tag{8}$$

The maximum duty cycle $D_{\max}$ is given by

$$D_{\max} = \frac{V_{\mathrm{dc2}} - V_{\mathrm{dc1min}}}{V_{\mathrm{dc2}}} \tag{9}$$

where V_{dc2} is the dc output voltage of the dc-to-dc converter ($V_{\mathrm{dc2}} = 500$ V) and V_{dc1min} is the minimum dc voltage of the uncontrolled rectifier.

The minimum dc voltage of the uncontrolled (V_{dc1min}) corresponds to the maximum voltage sag occurred in the

distribution system. Therefore V_{dc1min} can be given by

$$V_{dc1min} = 1 - D_{sag} V_{sL-L} \tag{10}$$

By substituting (10) into (9) and then the result is substituted in (8), the value of the inductor L_{dc} can be given by

$$L_{dc} = \frac{V_{sL-L}(V_{dc2} + D_{sag} V_{sL-L} - 1)}{\Delta I_{dc2} f_s V_{dc2}} \tag{11}$$

Fig. 8 illustrates the relation between the inductor L_{dc} and the voltage sag depth D_{sag}. It can be seen from Fig. 8 that as the D_{sag} increases the value of the inductor L_{dc} has to be increased. Since $D_{sag} = 0.5$ is selected in designing C_{fdc}, the value of the inductor L_{dc}, which corresponds to the same voltage sag depth, is selected to be $L_{dc} = 12$ mH.

Following the same procedure, the dc capacitor of the dc-to-dc step converter C_{dc} can be given by

$$C_{dc} = \frac{I_{dc2}(V_{dc2} + D_{sag} V_{sL-L} - 1)}{\Delta V_{dc2} f_s V_{dc2}} \tag{12}$$

The active power injected by the DVR during the voltage sag, ignoring the losses in the PWM converter, is given [14] by

$$P_{inj} = D_{sag} \frac{V_{sL-L}}{\sqrt{3}} I_L \cos \Phi = V_{dc2} I_{dc2} \tag{13}$$

The expression of the dc output current from the dc-to dc converter I_{dc2} can be obtained from (13) and then substituted in (12). Thus, the dc capacitor C_{dc} can be given by

$$C_{dc} = \frac{D_{sag} V_{sL-L} I_L \cos \Phi (V_{dc2} + D_{sag} V_{sL-L} - 1)}{\sqrt{3} \Delta V_{dc2} f_s V_{dc2}^2} \tag{14}$$

Fig. 9 shows the relation between the inductor C_{dc} and the voltage sag depth D_{sag} for various values of the power factor (cos Φ). It can be observed from Fig. 9 that voltage sag depth increases, the size of the dc capacitor C_{dc} should to be increased. Low power factor loads allow using lower value of the capacitor C_{dc} as can be seen from Fig. 9. For voltage sag depth $D_{sag} = 0.5$ and power factor of 0.8, the value of capacitor $C_{dc} = 30$ μF. It has to be mentioned that the size of C_{dc} is much smaller than the size of C_{fdc} since its main function is to reduce the ripple in the output dc voltage of the dc-to-dc step up converter V_{dc2} [12].

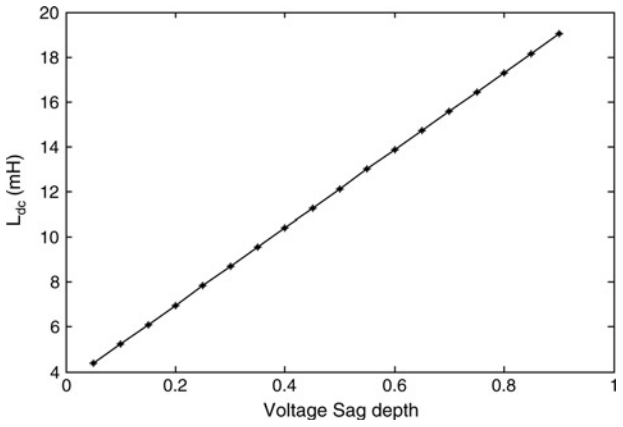

Figure 8 *Relation between inductor L_{dc} and voltage sag depth (D_{sag})*

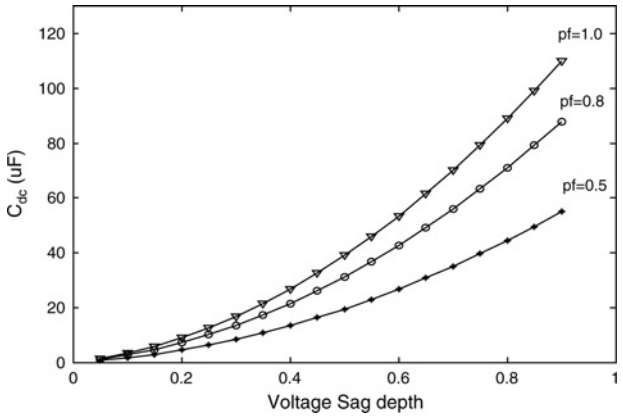

Figure 9 *Relation between capacitor C_{dc} and voltage sag depth (D_{sag})*

4 Time domain simulation

Four different situations are simulated, using MATLAB/SIMULINK and considering linear and non-linear loads, to verify the operation of the DVR proposed in this paper. These cases are:

1. Compensating 60% three-phase voltage sag with +28° phase jump only with linear and non-linear loads (Figs. 10 and 11).

2. Compensating supply voltage harmonics (fifth and seventh harmonics) only with linear and non-linear loads (Figs. 12 and 13).

3. Simultaneous compensation of 60% three-phase voltage sag with +28° phase jump and supply voltage harmonics (fifth and seventh harmonics) with linear and non-linear loads (Figs. 14 and 15).

4. Simultaneous compensation of 50% single-phase voltage sag with +28° phase jump and supply voltage harmonics (fifth and seventh harmonics) with linear and non-linear loads (Figs. 16 and 17).

The parameters of the test system are given in Appendix. The linear load considered in the simulation is an $R - L$ load ($R_L = 10.78\ \Omega$, $X_L = 0.808\ \Omega$) with 0.8

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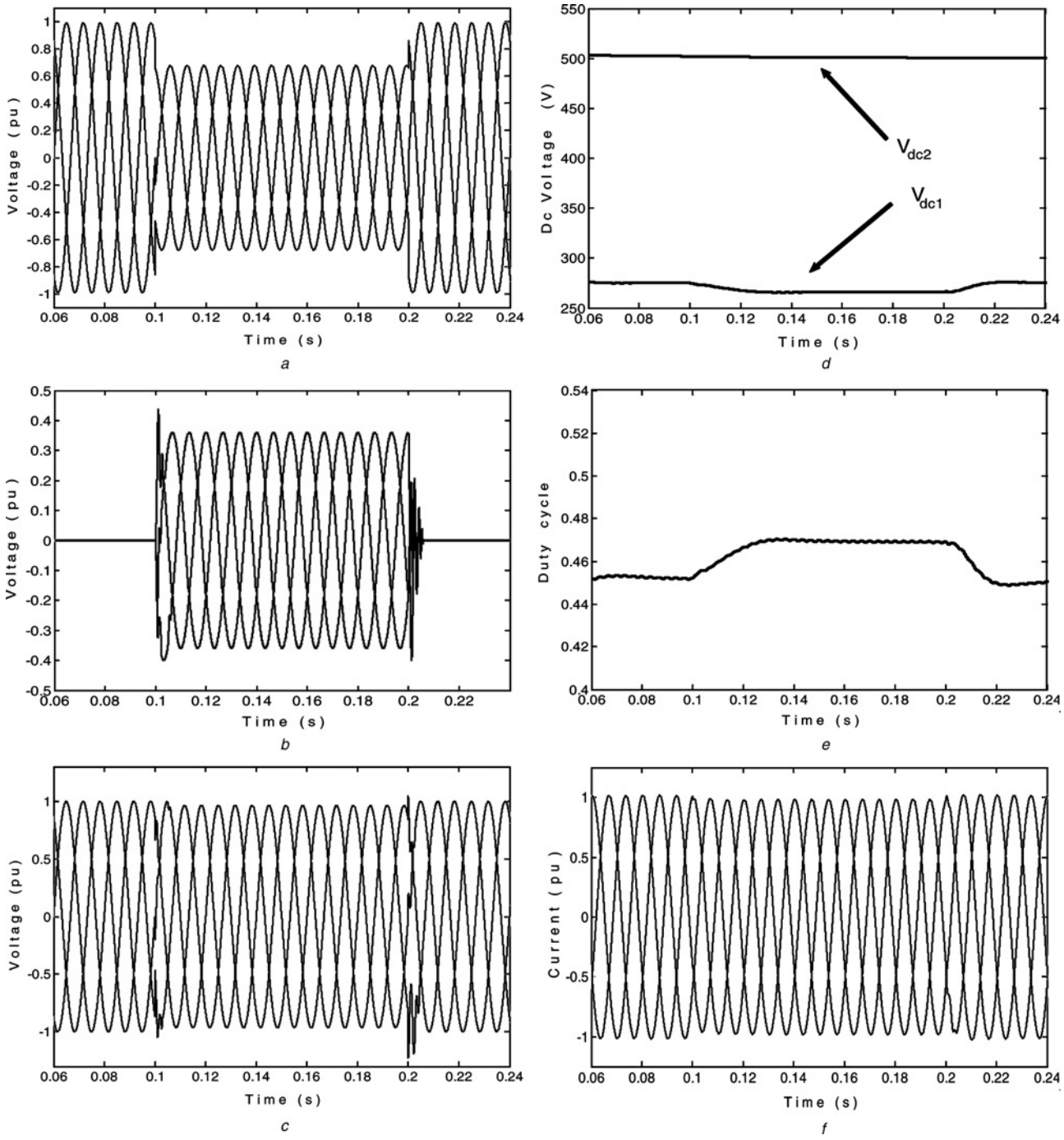

Figure 10 *System response because of three-phase 60% voltage sag with +28° phase jump (linear load)*

a Three-phase supply voltage
b Three-phase DVR voltage
c Three-phase load voltage
d Input and output dc voltages of the dc converter
e Duty cycle of the dc converter
f Three-phase load current

lagging power factor. Since the ability of the DVR to compensate harmonics is to be examined, the non-linear load is considered in the simulations. The non-linear load, which is shown in Fig. 2*b*, is a diode rectifier with parallel resistance/capacitive dc load. The value of the capacitance $C_{\mathrm{Ldc}} = 2000\,\mu\mathrm{F}$ and the resistor $R_{\mathrm{Ldc}} = 15\,\Omega$. In all figures produced in this section, the hysteresis band of the hysteresis voltage controller is $h = 0.000208$ pu.

Figs. 10 and 11 show, respectively, the response of the system because of 60% three-phase voltage sag with positive 28° phase jump considering linear and non-linear

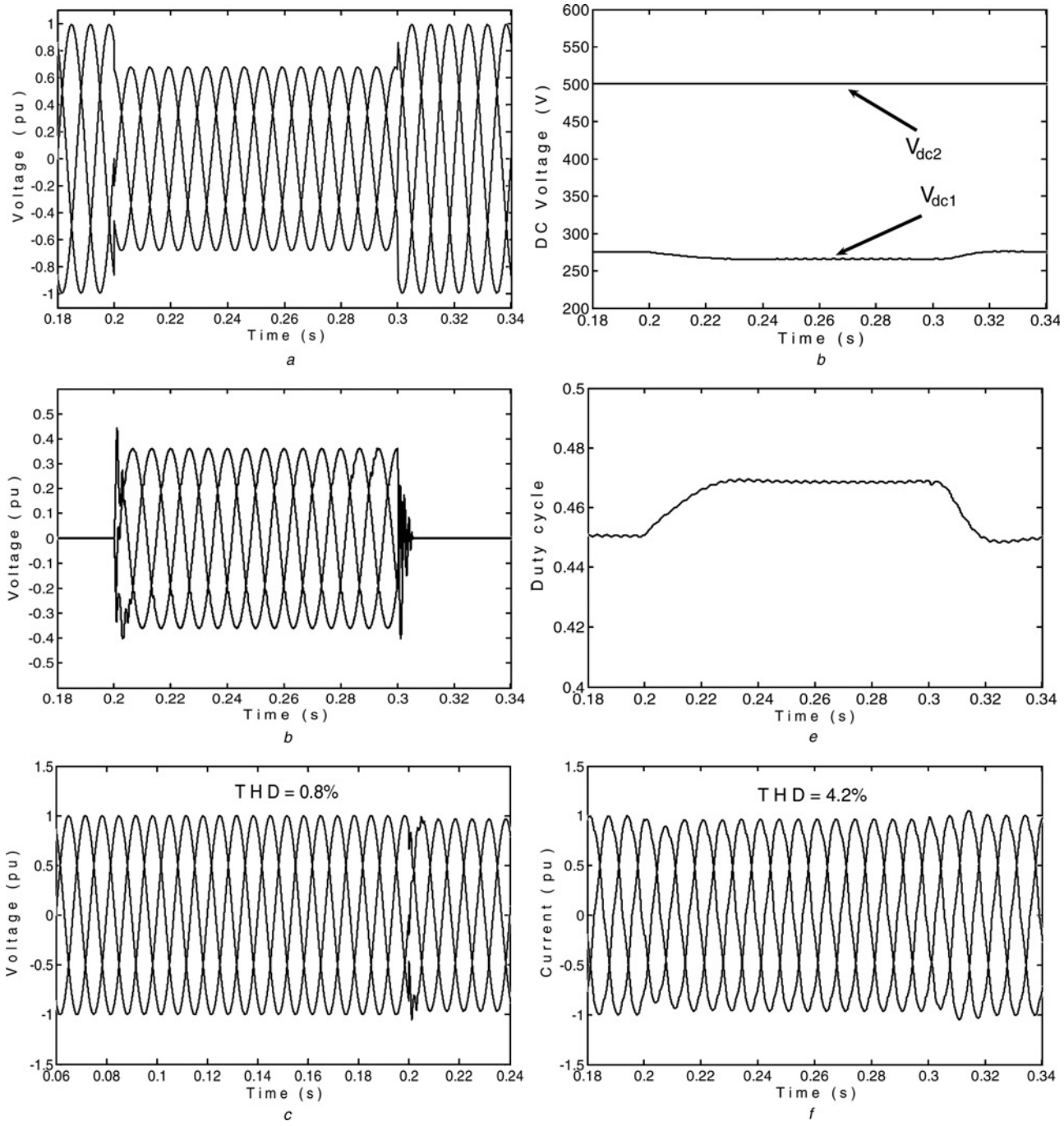

Figure 11 *System response because of three-phase 60% voltage sag with +28° phase jump (non-linear load)*

a Three-phase supply voltage
b Three-phase DVR voltage
c Three-phase load voltage
d Input and output dc voltages of the dc converter
e Duty cycle of the dc converter
f Three-phase load current

loads. It can be seen from Figs. 10*d* and 11*d* that when the supply voltage sags, the dc voltage of the three-phase rectifier (V_{dc1}) drops and stays constant at lower value. As a result of that, the PI controller reacts and increases the duty cycle D to keep the output voltage of the dc-to-dc converter constant at the reference setting value ($V_{dc2} = 500$ V) as depicted in Figs. 10*e* and 11*e*. As soon as the supply voltage is restored, the duty cycle D is returned to its pre-sag value.

Figs. 12 and 13 depict, respectively, the steady-state harmonics compensation capability of the DVR considering linear and non-linear loads. The fifth and seventh harmonics are added to the supply voltage to form a

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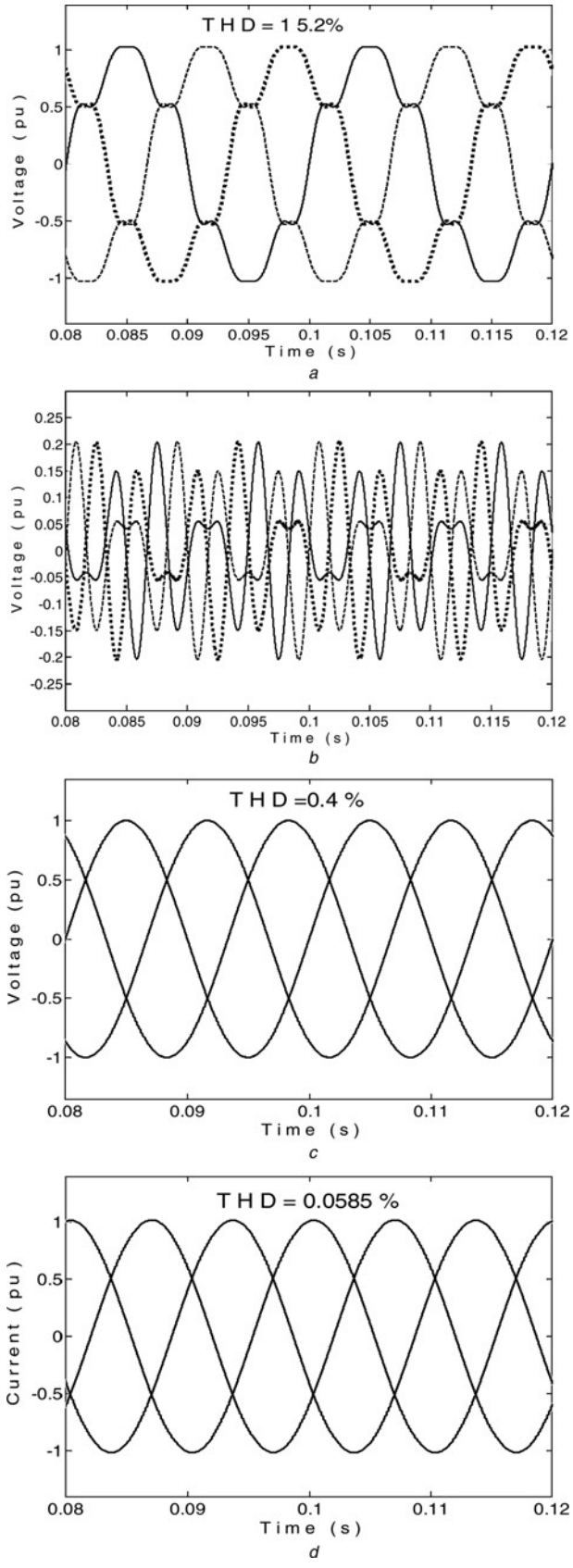

Figure 12 *Steady-state harmonic compensation (linear load)*

a Three-phase supply voltage
b Three-phase DVR voltage
c Three-phase load voltage
d Three-phase load current

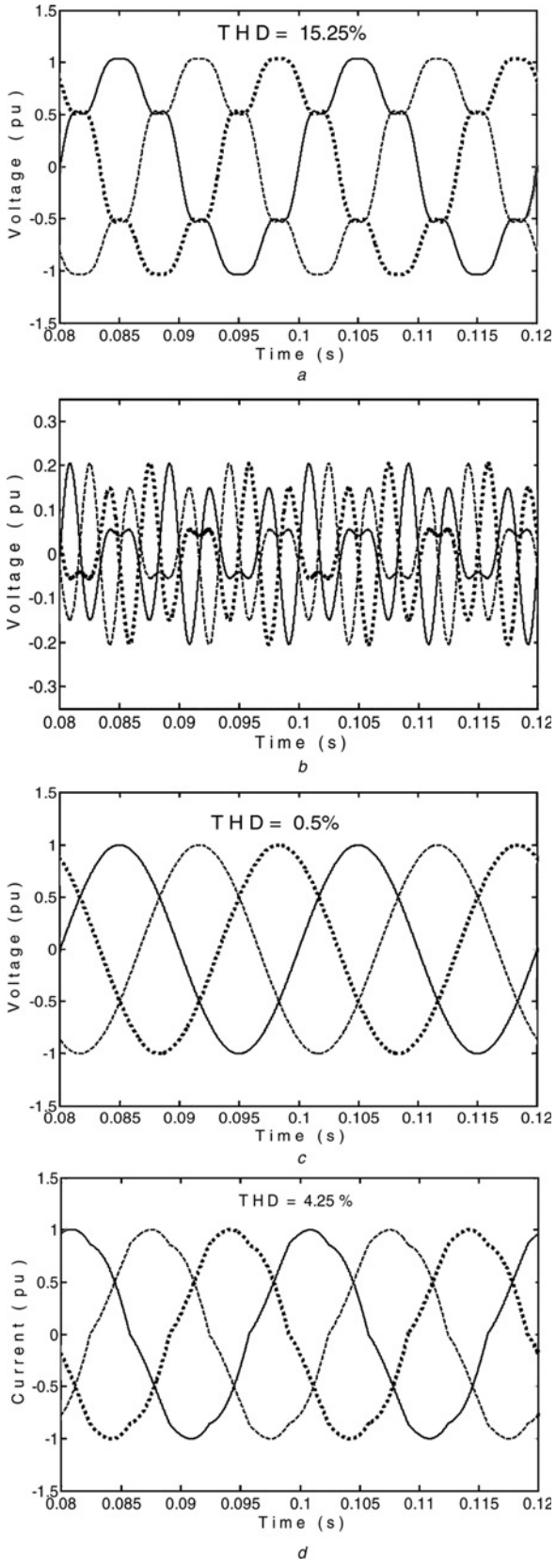

Figure 13 *Steady-state harmonic compensation (non-linear load)*

a Three-phase supply voltage
b Three-phase DVR voltage
c Three-phase load voltage
d Three-phase load current

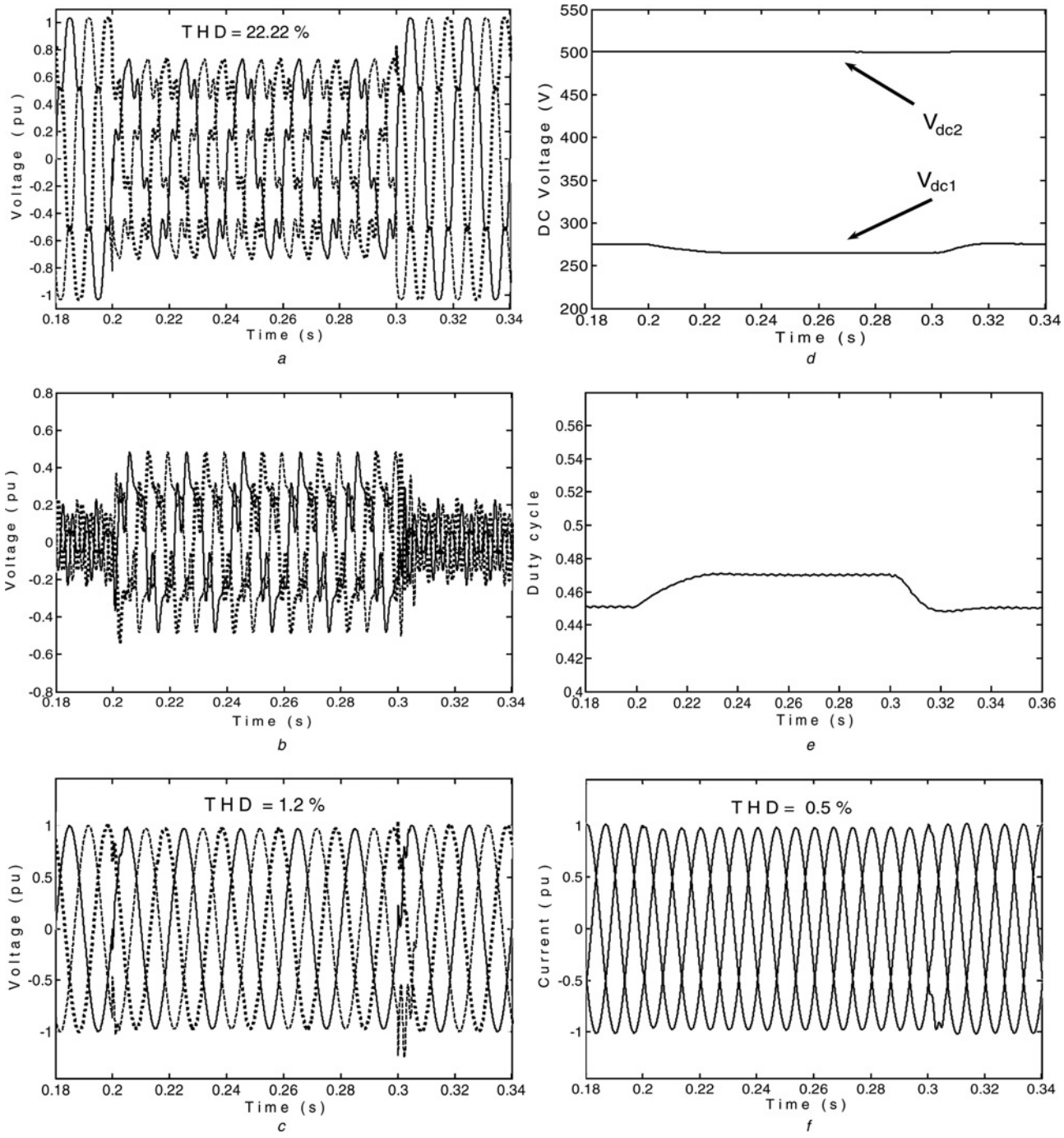

Figure 14 *Three-phase 60% voltage sag with +28° phase jump (linear load) and harmonic compensation*

a Three-phase supply voltage
b Three-phase DVR voltage
c Three-phase load voltage
d Input and output dc voltages of the dc converter
e Duty cycle of the dc converter
f Three-phase load current

distorted supply voltage. The magnitudes of the fifth and seventh harmonics are, respectively, 12.5 and 8.52% of the supply phase voltage. The total harmonic distortion (THD) in the supply voltage is 15.2% in both types of loads whereas the THD of the load voltage is 0.4% for linear load and 0.5% for non-linear load. This indicates that the DVR has substantially reduced fifth and seventh harmonics of the supply voltage.

Figs. 14 and 15 illustrate, respectively, simultaneous steady-state harmonics and voltage sag compensation capabilities of the DVR considering linear and non-linear

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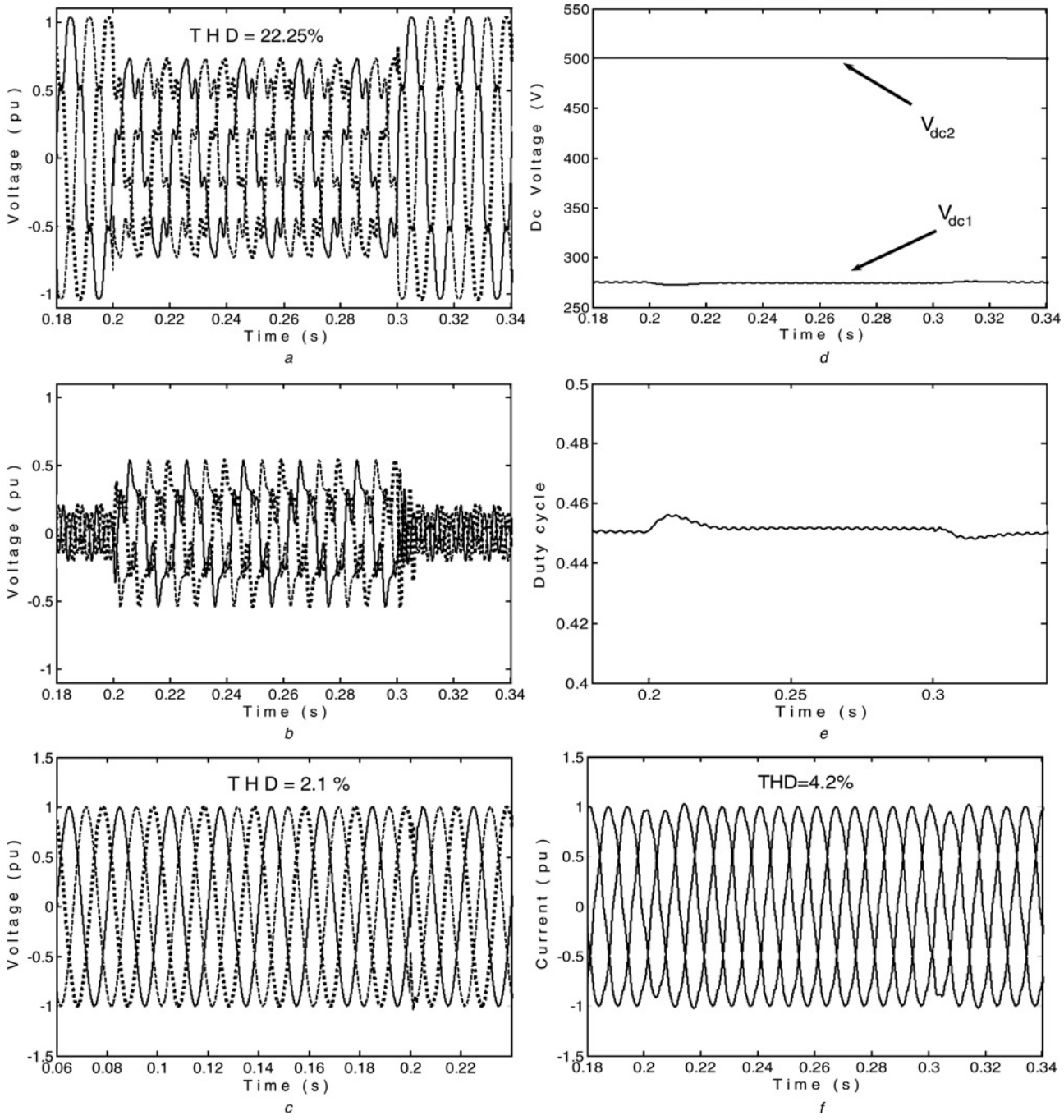

Figure 15 *Three-phase 60% voltage sag with +28° phase jump (non-linear load) and harmonic compensation*
a Three-phase supply voltage
b Three-phase DVR voltage
c Three-phase load voltage
d Input and output dc voltages of the dc converter
e Duty cycle of the dc converter
f Three-phase load current

loads for 60% three-phase voltage sag with +28° phase jump. The magnitudes of the fifth and seventh harmonics are, respectively, 12.5 and 8.52% of the supply phase voltage which are held constant during the voltage sag to consider worst-case scenario. The THD in the supply voltage is 22.22% in both loads whereas the THD of the load voltage is 1.2% for linear load and 2.1% for non-linear load during the voltage sag. It can be seen that the harmonic compensation of the DVR continues to function and at the same time the DVR is capable of compensating the three-phase voltage sag.

It can bee seen from Figs. 11*f*, 13*d* and 15*f* that the THD of the load current is 4.2% with non-linear load. The THD

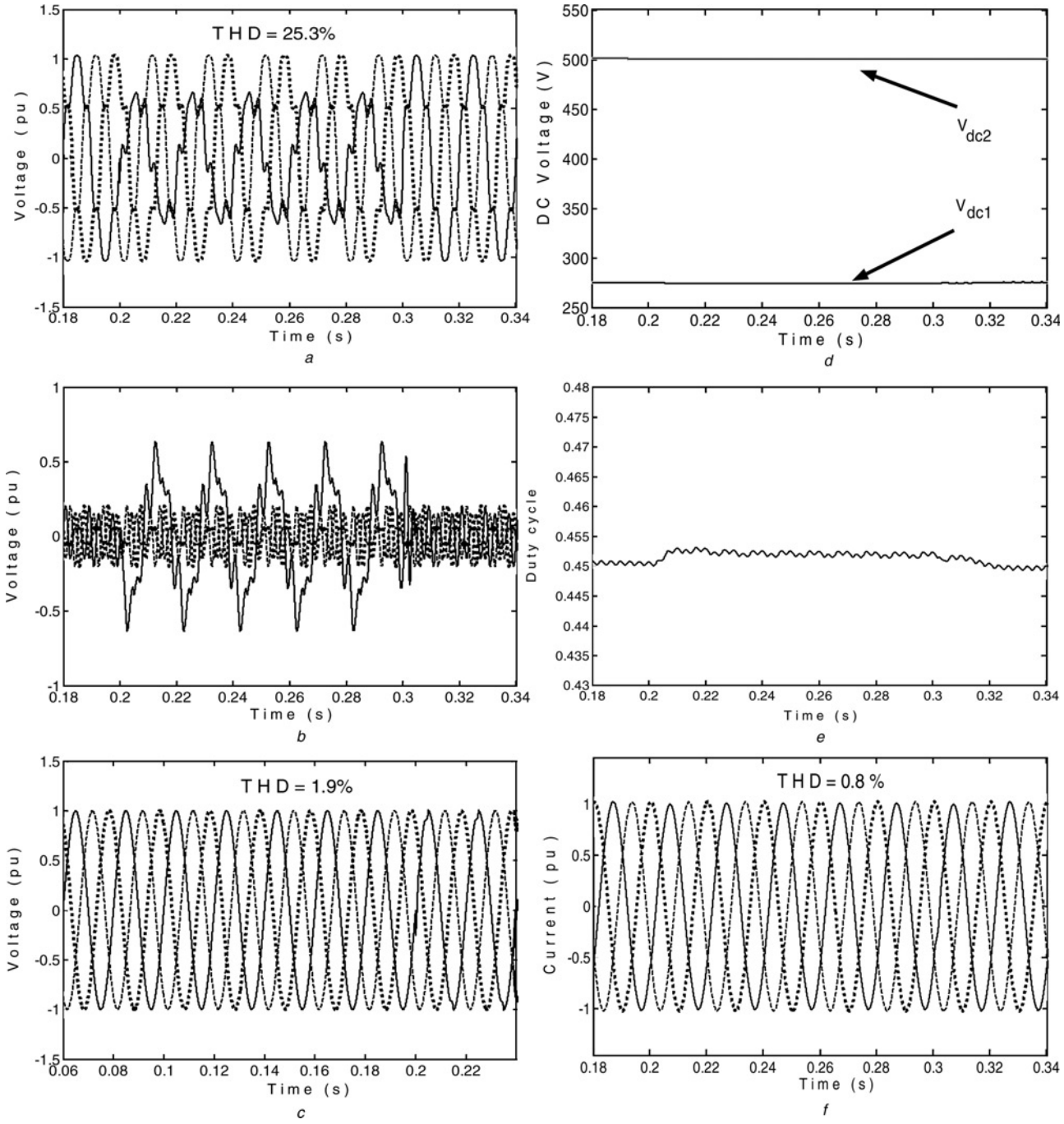

Figure 16 *Single-phase 50% voltage sag with +28° phase jump (linear load) and harmonic compensation*

a Three-phase supply voltage
b Three-phase DVR voltage
c Three-phase load voltage
d Input and output dc voltages of the dc converter
e Duty cycle of the dc converter
f Three-Phase load current

of the load current can be reduced by adding an inductor in series with the non-linear load [9].

Figs. 16 and 17 show, respectively, simultaneous steady-state harmonics and voltage sag compensation capabilities of the DVR considering linear and non-linear loads for 50% single-phase voltage sag with +28° phase jump. This simulation test is performed to validate the design of the components, presented in Section 5, since they are designed based on 50% single-phase voltage sag. It can be seen from Figs. 16 and 17 that there is almost no fluctuation in the dc voltage of the shunt rectifier V_{dc1} and the output dc voltage of the dc-to-dc step up converter V_{dc2}.

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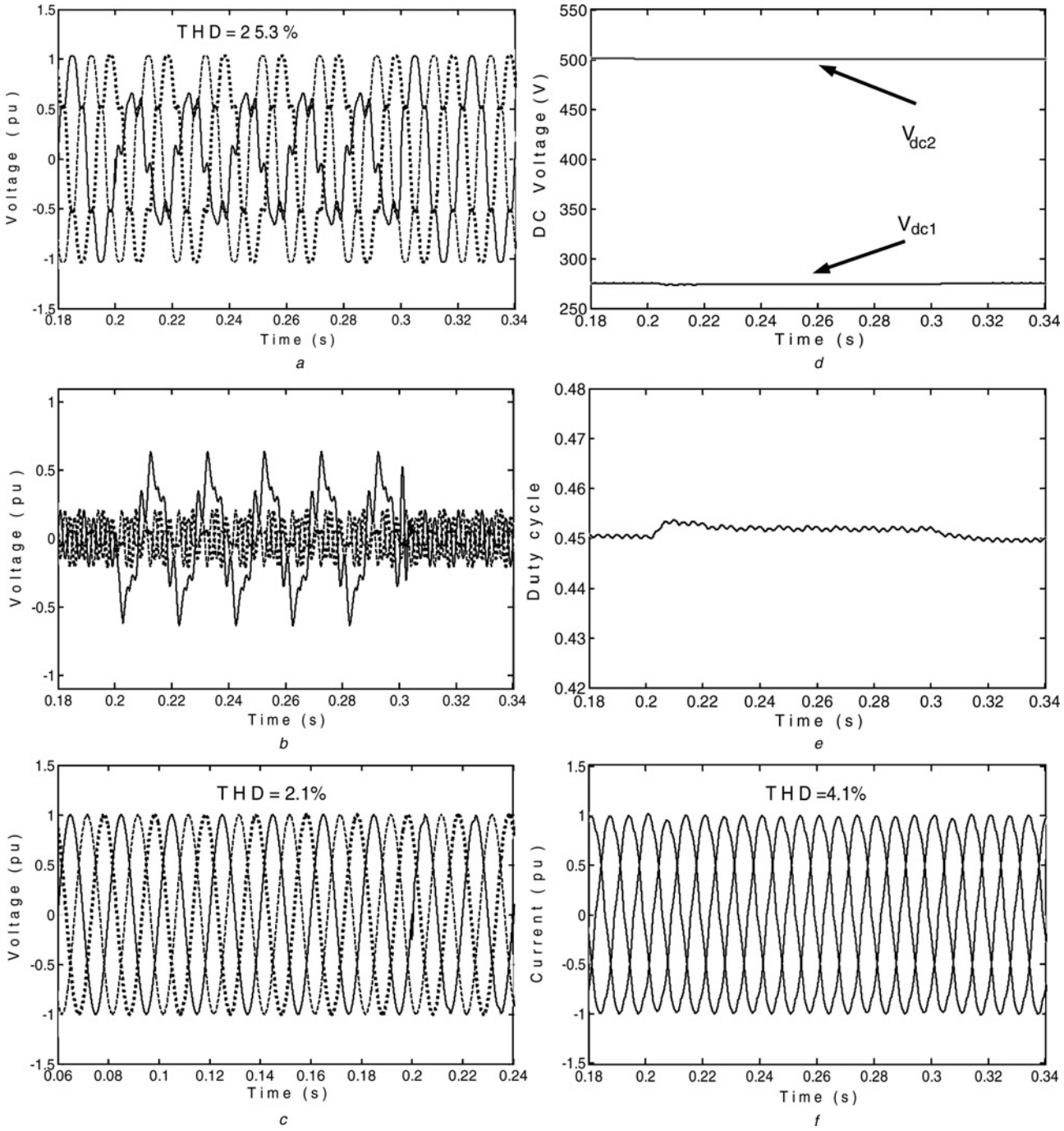

Figure 17 *Single-phase 50% voltage sag with +28° phase jump (non-linear load) and harmonic compensation*

a Three-phase supply voltage
b Three-phase DVR voltage
c Three-phase load voltage
d Input and output dc voltages of the dc converter
e Duty cycle of the dc converter
f Three-phase load current

5 Conclusion

This paper has proposed a DVR that can compensate deep and long duration voltage sag and, simultaneously, compensate steady-state harmonics. The DVR is based on a shunt rectifier fed series inverter through dc-to-dc step up converter. A method of incorporating harmonic compensation capability to the DVR has been proposed using hysteresis voltage control. The design of the components of the DVR has been presented. The influence of the power factor of the load and the depth of the voltage sag on the size of the dc capacitor of the shunt rectifier and the inductor and dc capacitor of the dc-to-dc step up converter has been analysed. It has been shown that higher power factor loads require higher dc capacitor size

for both; the shunt rectifier and the dc-to-dc step up converter. In addition, it has been shown that as the depth of the voltage sag increases, the size of dc capacitors of shunt rectifier and the dc-to dc step up converter as well as the size of the inductor of the dc-to-dc step up converter have to be increased. Time domain simulations of the DVR, under different conditions including distorted supply voltage and distorted voltage sags, have validated the operation of the proposed DVR.

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7 Appendix

1. Power supply: $V_{sL-L} = 415$ V, $f = 50$ Hz

2. Dc-to-dc step-up converter: $L_{dc} = 12$ mH, $C_{dc} = 30\,\mu$F DC voltage control: $K_p = 0.06$, $K_i = 0.9$. $D_{max} = 0.8$ and $D_{min} = 0.15$.

3. Series transformer $240V_{phase}/240V_{phase}$, $r_1 = r_2 = 0.004$ pu, $x_1 = x_2 = 0.08$ pu

4. Shunt transformer: $240V_{phase}/120V_{phase}$, $r_1 = r_2 = 0.004$ pu, $x_1 = x_2 = 0.08$ pu

5. DC link capacitor: $C_{fdc} = 200\,\mu$F

6. RC-AC filter: $R_{fac} = 1\,\Omega$, $C_{fac} = 50\,\mu$F

7. Sensitive load:

i. Linear load: $R_L = 10.78\,\Omega$, $X_L = 0.808\,\Omega$.

ii. Non-linear load: $R_{Ldc} = 15\,\Omega$, $C_{Ldc} = 2000\,\mu$F.

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