Harmonic Reduction Technique with a Five-level Inverter for Four Pole Induction Motor Drive

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***Abstract*—In this paper a five-level inverter topology is presented for a four pole induction motor drive with a single DC source. In any ac motor, the winding coils which are 360^0 (electrical) apart will have identical voltage profiles. A conventional four pole induction machine consists of two such Identical Voltage Profile Winding Coils (IVPWCs) which are connected in series (or parallel). In the proposed method the series (or parallel) connected IVPWCs are disconnected into two parts. Each IVPWC is fed by a two two-level inverters from both the sides thereby four two-level inverters are used to generate the five-level voltage across the motor phase winding. All these four two-level inverters are connected to the same DC source with a magnitude $\frac{V_{dc}}{4}$ (where V_{dc} is the dc bus voltage required for conventional five-level NPC inverter). Pulses for this five-level inverter configuration is generated using Unipolar phase shifted carrier PWM (UPSC PWM) technique by providing appropriate phase shift between modulating waves and carrier waves independently. Using the advantage of both IVPWCs of the induction motor stator winding and UPSC PWM the harmonics can be shifted to higher order which is close to four times compared to the harmonics with general SPWM. This circuit configuration does not require any major design modifications of the induction motor except the disconnection between the IVPWCs. The five-level inverter configuration supplying a 5hp four pole induction motor drive is tested with unipolar phase shifted carrier PWM in MATLAB(Simulink). Although the work is carried with 5hp induction motor, results are similar for large machines also.**

***Index Terms*—Five-level Inverter, Induction Motor Drive, UPSC PWM.**

I. Introduction

NOWADAYS, demand for the inverter fed ac drives is increasing significantly. The variable speed ac drives require variable voltage and variable frequency to control the rotor speed without disturbing the air gap flux magnitude. To provide the variable voltage and variable frequency generally inverters are preferred. But an inverter generates output voltage with required fundamental component along with considerable harmonic content. So these harmonics will cause to increase the losses in the machine. Therefore the reduction of harmonics is the major concern in any power converter fed ac drives. These harmonics can be minimized by using some Pulse Width Modulation (PWM) Techniques. The role of the PWM Technique is for controlling the output voltage and frequency of the inverter and also to minimize the harmonic content of the inverter output voltage [1]-[4]. Many PWM techniques have been presented to minimize the harmonic content in the inverter output voltage. One of the basic harmonic elimination techniques, selective harmonic elimination method presented in [5] deals with the harmonic minimization by properly defining the switching angles with the help of distribution ratio. But more off-line calculations are needed which increases the complexity of the system as the number of levels are increased. An interesting PWM technique presented in [6] considering trapezoidal modulating wave and the sinusoidal carrier wave with variable frequency, where the harmonic content is minimized by varying the frequency of the carrier signal with the slope of the trapezoidal modulating wave. A survey of eight different advanced PWM techniques are presented in [7], where the advantages and disadvantages of each method are discussed in terms of complexity and implementation.

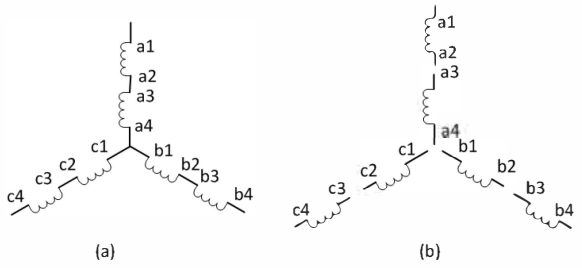

Fig. 1. Induction Motor stator winding, (a) General winding arrangement (b) Winding arrangement for the proposed inverter

On the other hand harmonic profile of the output voltage can be improved by using multi-level inverters. Many multilevel inverter configurations are proposed in the literature to improve the harmonic spectrum of the output voltage [8]-[9]. The basic concept of multi-level inverters is, connecting power electronic switches in series/parallel along with more number of DC sources to synthesize the staircase waveform. This small stepped staircase waveform will result in better output waveform quality and lower voltage stress on the power electronic devices. One of the popular and basic multi-level inverter topology is a diode clamped (or NPC) multi-level inverter [10]. Although better voltage waveform can be achieved with the NPC inverter, it requires more number of clamping diodes and also there are some issues with the capacitor voltage unbalancing. So the special voltage balancing technique is required to maintain equal voltages across the capacitors. Another conventional topology is the flying capacitor (or capacitor clamped) multi-level inverter [11]. This topology does

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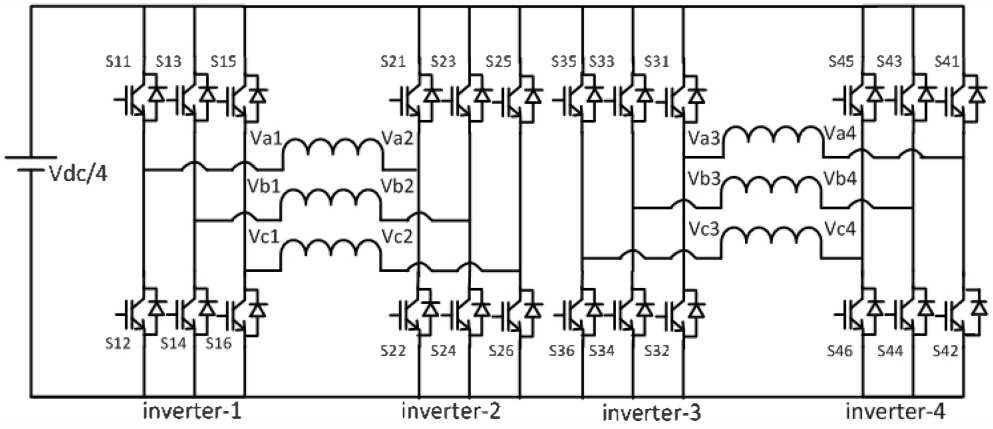

Fig. 2. Five-level inverter Topology

not require any clamping diodes, but it requires more number of capacitor banks. These capacitor bank voltages should be controlled within allowable voltage ripple. An interesting topology without capacitor voltage unbalancing issues and clamping diodes is a cascaded H-bridge inverter [12]. But it requires more number of isolated DC voltage sources. The multi-level voltage waveform can also be achieved with two two-level inverters by feeding the induction motor winding from both the sides [13]-[14]. This will reduce the dc source voltage requirement to half, compared to the conventional multi-level inverters.

In this paper a five-level inverter topology is derived by using the concept of IVPWCs. The winding coils which are 360^0 (electrical) apart in any ac motor winding will have identical voltage profiles. Therefore a conventional four pole induction motor consists of two IVPWCs per phase (where the number of IVPWCs is equal to half the number of poles) [8]. These two windings are connected in series in a conventional induction motor as shown in Fig.1(a). But for the present work these two windings are disconnected at middle of the each phase winding and it is shown in the Fig.1(b). These four terminals are fed by four two-level inverters and these four inverters are switched in such a way that equal average voltage should be applied across each IVPWC.

In order to shift the harmonics to higher order, UPSC PWM [16]-[18] is used in the present work. From this PWM technique it can be noticed that harmonics can be shifted to the higher levels by providing phase shift between the modulating waves and the carrier waves independently. By providing 180^0 phase shift between modulating waves, harmonics at all odd center bands (first center band, third center band, etc..) will be cancelled. By providing 90^0 phase shift between the carrier waves, harmonics at second center band will be cancelled which will be explained in detail in section-III. By using the above mentioned PWM technique and disconnected IVPWCs of the induction motor, harmonics are shifted to higher levels compared to the conventional sine-triangle PWM controlled induction motor.

II. Five-Level Inverter Configuration

The Five-level inverter topology is derived by using the concept of IVPWCs of the induction motor. The two IVPWCs of the four pole induction motor are disconnected and each IVPWC is fed with two two-level inverters from both the sides. Thereby four two-level inverters are used to feed the two IVPWCs. All these four inverters are connected to the same DC source with magnitude of $\frac{V_{dc}}{4}$ as shown in the Fig. 2. In all four two-level inverters, each leg consists of two switches which are complimentary to each other (i.e. during the conduction of one switch the other switch should be off). In the Fig. 2, inverter-1 and inverter-2 together feeding one IVPWC. Similarly the inverter-3 and inverter-4 are feeding another IVPWC. Because of the winding disconnection exactly at middle, both the windings have equal number of turns (conductors), which acknowledges that both the windings have the equal resistance, equal self-inductance and equal magnetizing-inductance which are equal to the half of the conventional induction machine parameters [19]. Since the resistance, self-inductance and magnetizing-inductance of each IVPWC is half of the conventional induction motor, the voltage magnitude required to excite each IVPWC is half of the rated voltage required to excite the conventional induction motor. Similarly the winding is fed from both sides, again the dc voltage requirement is reduced to half. Therefore dc voltage requirement is $\frac{1}{4}^{th}$ compared to conventional NPC or Flying capacitor five-level inverter.

When compared with the conventional topologies the proposed topology does not require any clamping diodes, any capacitor banks and it requires only one dc source with magnitude of $\frac{V_{dc}}{4}$ only. Using the proposed topology harmonics are shifted four times compared to the conventional topologies which will be explained in the next section.

III. Unipolar Phase shifted carrier Pulse Width Modulation (UPSC PWM)

In this unipolar phase shifted carrier PWM, two modulating waves which are phase shifted by 180^0 from each other and one carrier wave (carrier wave-1) are used to generate the pulses for inverter-1 and inverter-2 as shown in Fig. 2. For

better understanding, A-phase winding and associated inverter leg connection of the proposed topology is shown in Fig. 3. The modulating wave-1 (shown in the Fig. 4) is compared with the carrier wave-1 and pulses are generated for the first inverter (inverter-1 shown in the Fig. 3) as follows

$$\begin{aligned} \text{If} \quad V_M > V_{CR} \quad &\text{then} \quad S_{11} \quad \text{is} \quad ON \\ &\text{else} \quad S_{12} \quad \text{is} \quad ON \end{aligned}$$

The modulating wave-2 which is phase shifted by 180^0 from the modulating wave-1, (shown in the Fig. 4) is compared with the same carrier wave-1 and pulses are generated for the second inverter (inverter-2 shown in Fig. 3) as follows

$$\begin{aligned} \text{If} \quad V_M > V_{CR} \quad &\text{then} \quad S_{21} \quad \text{is} \quad ON \\ &\text{else} \quad S_{22} \quad \text{is} \quad ON \end{aligned}$$

Since the inverter-1 and inverter-2 are connected to the same DC source and modulating wave-2 is phase shifted by 180^0 from the modulating wave-1, the output voltage that is appearing at V_{A2} is equal in magnitude with V_{A1} but opposite in direction (i.e., $V_{A1} = -V_{A2}$). Therefore the total average voltage appearing across first IVPWC is the difference between V_{A1} and V_{A2} (i.e., $V_{A12} = V_{A1} - V_{A2}$).

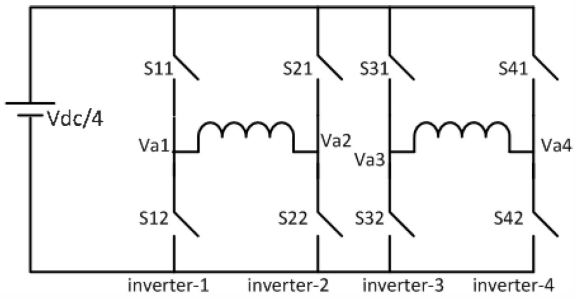

Fig. 3. Schematic diagram of 1-ϕ representation.

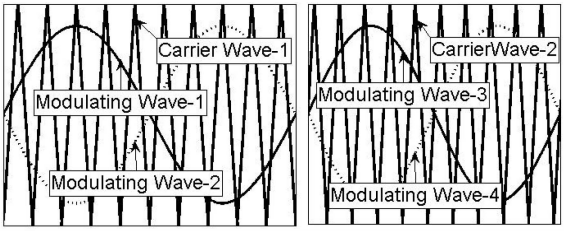

Fig. 4. Sinusoidal Unipolar Pulse Width Modulation.

Pulses for the inverter-3 and inverter-4 are generated with the help of two modulating waves having phase shift 180^0 from each other and one carrier wave (carrier wave-2) having 90^0 phase shift from the carrier wave-1 (shown in Fig. 4). The remaining procedure for generating pulses to the inverter-3 and inverter-4 (shown in fig.3) is same as above (as explained for the inverter-1 and inverter-2). Since the inverter-3 and inverter-4 are connected to the same DC source and modulating wave-4 is phase shifted by 180^0 from the modulating wave-3, the output voltage that is appearing at V_{A4} is equal in magnitude with V_{A3} but opposite in direction (i.e., $V_{A3} = -V_{A4}$). So the total voltage appearing across the second IVPWC is the difference between V_{A3} and V_{A4} (i.e., $V_{A34} = V_{A3} - V_{A4}$).

Since the modulating signals of the inverter-1,inverter-2 and the inverter-3,inverter-4 are identical, the average voltage appearing across both the IVPWCs are equal in magnitude and polarity. Thereby the average output voltage appearing across the total motor phase winding is equal to the sum of the average voltage appearing across the two IVPWCs. Because of the 90^0 phase shift between the carrier wave-1 used for the inverter-1 (inverter-2) and the carrier wave-2 used for the inverter-3 (inverter-4), five level output voltage wave form will be produced across the motor phase winding. The harmonics at all odd center bands are cancelled by providing 180^0 phase shift between the modulating waves. Similarly the harmonics at second center band are cancelled by providing 90^0 phase shift between these carrier waves.

IV. Results and Discussion

The proposed five-level inverter topology feeding four pole induction motor drive is simulated in MATLAB (Simulink). The gating pulses are generated using UPSC PWM technique and given to each 3-phase two-level inverters individually. The switching frequency is kept constant at 1kHz and the modulating wave frequency is changed. The voltage across the first and second IVPWC are $(V_{a1} - V_{a2})$ and $(V_{a3} - V_{a4})$ respectively and the total average voltage across the stator winding is the sum of the voltages across the two IVPWCs which is equal to $(V_{a1} - V_{a2})$+$(V_{a3} - V_{a4})$. The voltage across each IVPWC, total average voltage across the stator winding, stator current (I_a) and the harmonic spectrum of sine-triangle PWM are presented for the modulation index of 0.2, 0.4, 0.6 and 0.8. Fig. 5 and Fig. 6 demonstrate the results for the

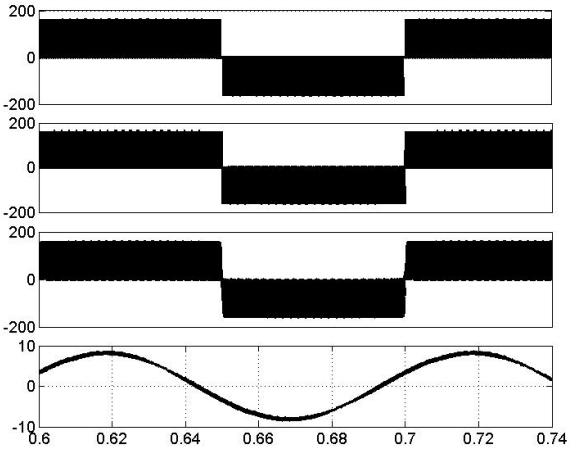

Fig. 5. Top trace is the voltage across the first IVPWC. Second trace is the voltage across the second IVPWC. Third trace is the effective voltage across the motor phase winding. Bottom trace is the stator current (I_a) for modulation index=0.2.

modulation index 0.2 (where the modulation index is equal to the ratio of peak of the modulating signal to peak of the carrier signal). Here the fundamental frequency is 10Hz and the frequency modulation ratio (m_f) is 100 (where the frequency modulation ratio is defined as the ratio of switching

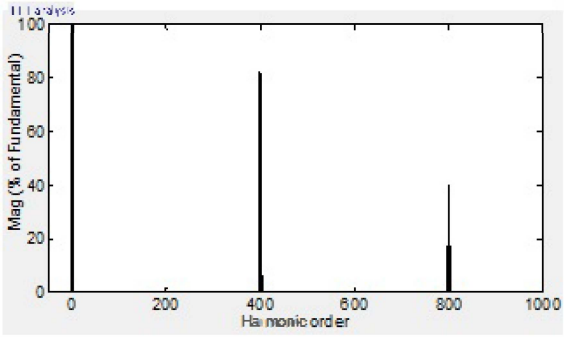

Fig. 6. Harmonic spectrum for the modulation index = 0.2.

frequency to the fundamental frequency). From the harmonic spectrum shown in Fig. 6, it is clear that all the lower order harmonics are shifted to four times the m_f which reveals that the harmonics at this level does not have any impact on the motor phase windings.

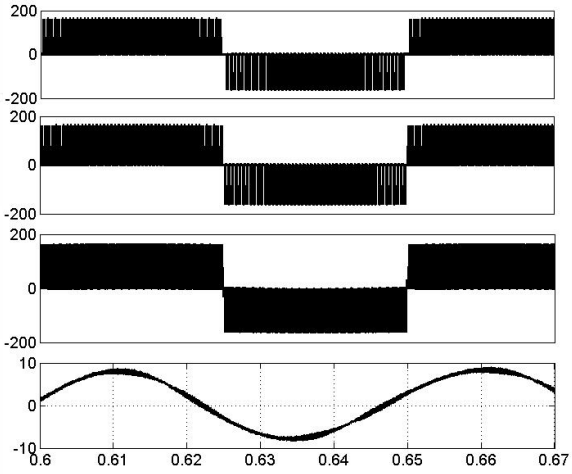

Fig. 7. Left side Top trace is the voltage across the first IVPWC. Second trace is the voltage across the second IVPWC. Third trace is the effective voltage across the motor phase winding. Bottom trace is the stator current (I_a)for the modulation index = 0.4.

Results for the modulation index 0.4 are shown in the Fig. 7 and Fig. 8, where fundamental frequency is 20Hz and the frequency modulation ratio is 50. Harmonic spectrum shown in Fig. 8 acknowledges that all the lower order harmonics are shifted to 200^{th} harmonic level which is equal to the four times of the m_f. From the third top trace of the Fig. 5 and Fig. 7 it is clear that, for the modulation index less than 0.5, the proposed inverter configuration will be operated as a three-level inverter. Results corresponding to the modulation index 0.6 were shown in the Fig. 9 and Fig. 10 which has fundamental frequency of 30Hz and frequency modulation ratio of 33.3. From the results shown in Fig. 10 reveal that all the lower order harmonics are shifted to 133^{rd} harmonic level which is equal to four times the $\mathrm{m_f}$. Fig. 11 and Fig. 12 illustrate the results for the modulation index 0.8 where the frequency modulation ratio is 25 corresponding to the fundamental frequency 40Hz. From the harmonic spectrum of Fig. 12 it is clear that all the lower order harmonics are shifted to 100^{th} harmonic level which

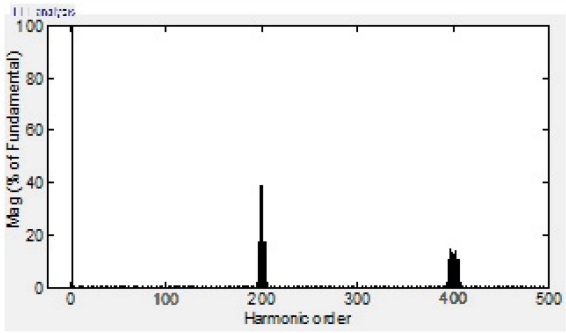

Fig. 8. Harmonic spectrum for the modulation index = 0.4.

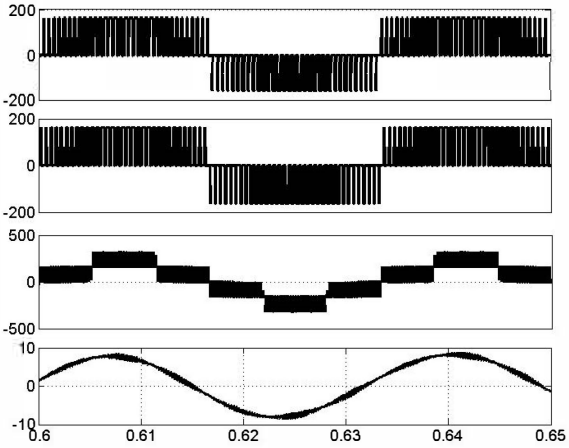

Fig. 9. Left side Top trace is the voltage across the first IVPWC. Second trace is the voltage across the second IVPWC. Third trace is the effective voltage across the motor phase winding. Bottom trace is the stator current (I_a)for the modulation index = 0.6.

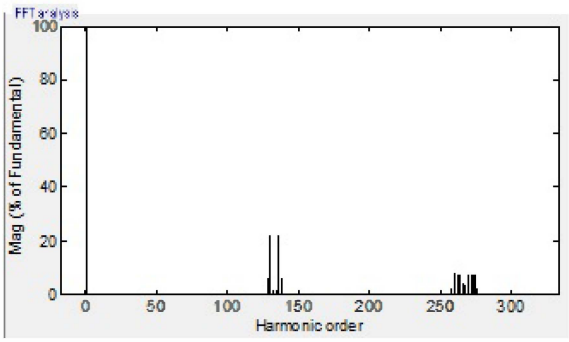

Fig. 10. Harmonic spectrum for the modulation index = 0.6.

is equal to four times the (m_f). From the third top trace of the Fig. 9 and Fig. 11 it can be observed that for the modulation index greater than 0.5, the circuit configuration will be operated as a five-level inverter. Harmonic spectrum for the voltage across one IVPWC is shown in Fig. 13. From Fig. 13 it can be noticed that the harmonics at all odd center bands will be cancelled by providing 180^0 phase shift between two modulating waves.

From the simulation results it is concluded that harmonics were shifted to four times the switching frequency by providing 180^0 phase shift between modulating waves and 90^0 phase

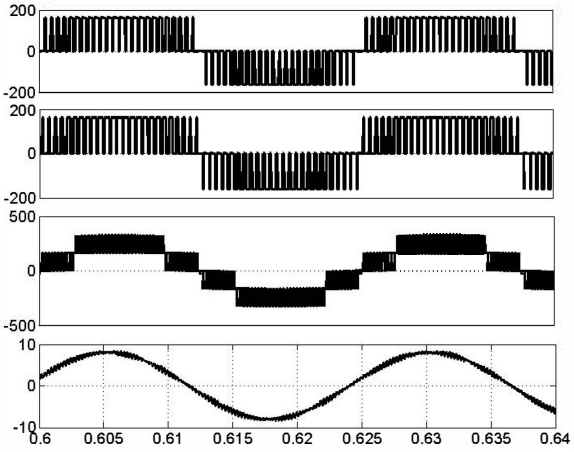

Fig. 11. Left side Top trace is the voltage across the first IVPWC. Second trace is the voltage across the second IVPWC. Third trace is the effective voltage across the motor phase winding. Bottom trace is the stator current (I_a)for the modulation index = 0.8.

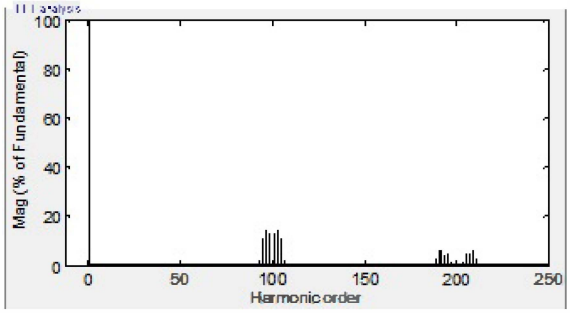

Fig. 12. Harmonic spectrum for the modulation index = 0.8.

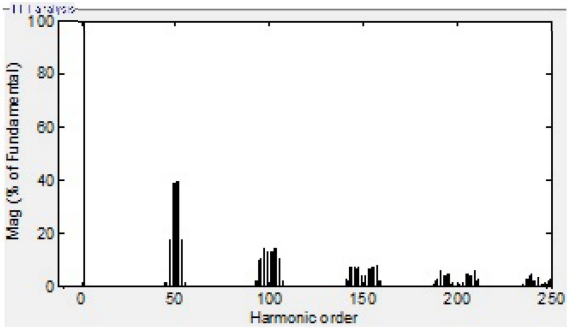

Fig. 13. Harmonic spectrum of the voltage across one IVPWC.

shift between carrier waves. The proposed five-level inverter configuration can be operated in complete linear modulation region with UPSC PWM technique.

V. Conclusion

In this paper a five-level inverter configuration for four-pole induction motor drive was presented. The two IVPWCs of the four pole induction motor were disconnected and each IVPWC was fed with two two-level inverters from both sides. All these two-level inverters were connected to the same dc source and the dc voltage requirement is reduced to $\frac{1}{4}^{\text{th}}$ of the conventional five-level NPC inverter. Capacitor voltage unbalancing issue is avoided, because this configuration is using only two-level inverters. The UPSC PWM was used to generate the pulses for all two-level inverters by providing proper phase shift between the modulating waves and the carrier waves independently. The proposed topology was simulated in MATLAB (Simulink) with 5hp four pole induction motor using UPSC PWM technique. Using the advantage of both disconnected IVPWCs of the induction motor and UPSC PWM, the harmonics were shifted to four times higher level compared to the harmonics with conventional SPWM. From this it can also be observed that the switching frequency of the inverters can be reduced which gives to the reduction in the switching losses. The five-level output voltage was produced because of the 90^0 phase shift between the carrier waves. Although this simulation is carried for four pole induction motor, this can be extended to any number of poles. As the number of poles increases the output voltage levels will be increased and the harmonics also will be shifted to number of poles times the switching frequency.

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