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Topology and Capacitor Voltage Balancing Control of a Symmetrical Hybrid Nine-Level Inverter for High Speed Motor Drives

Kui Wang, Zedong Zheng, Dabo Wei, Boran Fan, Yongdong Li
State Key Lab of Power System, Dept. of Electrical Engineering
Tsinghua University
Beijing, China
wangkui@tsinghua.edu.cn

***Abstract*—In order to increase the output voltage levels and reduce the isolated DC sources, a symmetrical hybrid nine-level inverter for high speed motor drive applications is presented in this paper. Each phase of this inverter is composed of a five-level DC/DC converter cell and an H-bridge cell. The DC/DC converter is operated at high frequency with low voltage devices and the H-bridge is operated at fundamental frequency with high voltage devices. The three phases are connected to a common DC-link and each drives an isolated winding of an open-winding motor. The operating principles and modulation method is introduced. A detailed analysis of the average currents through the flying capacitor and neutral point of the DC-link is presented and a capacitor voltage balancing method based on phase-shifted PWM is proposed. Simulation and experimental results are presented to demonstrate the feasibility of this topology and control method.**

Index Terms--multilevel converter; symmetrical hybrid; nine-level; capacitor voltage balancing; phase-shifted PWM; high speed motor

I. INTRODUCTION

Multilevel converters have been widely used in high voltage high power and high frequency applications since 1980s [1]–[4]. Plenty of multilevel topologies have been developed and among them, neutral-point-clamped (NPC), flying-capacitor (FC) and cascaded H-bridge (CHB) multilevel converters are three classical and basic multilevel topologies which are the most widely used in the industry [5]–[8].

Three-level NPC converter is widely used in medium-voltage (1.14, 2.3, 3.3 and 4.16 kV) applications [6]. Limited by the present semiconductor blocking voltage ratings, 3L-NPC converter is hard to be applied in high voltage drives over 6 kV. Although five-level NPC converter is a choice in this case, it suffers from the voltage imbalance of dc-link capacitors and requires mass clamping diodes [9].

Flying-capacitor multilevel converter is another topology suitable for high power applications [7]. By properly using the redundant switching states, the voltages across all the flying capacitors can be balanced [10]–[14]. However, the number of clamping capacitors in this converter increases rapidly with the voltage level, which increases the system volume, weight and control complexity tremendously.

Cascaded H-bridge (CHB) converter is another commercialized multilevel topology for 6 kV, 10kV or even higher voltage applications [8]. In order to increase the voltage levels, a large number of H-bridge cells are connected in series and powered by isolated DC sources. A multi-winding transformer with a number of isolated secondary windings is often used, which is huge, complex and expensive.

In order to increase the voltage levels and reduce the number of clamping devices and isolated DC sources, plenty of new multilevel topologies have been proposed based on the combination of different types of multilevel topologies, which is classified as hybrid multilevel topologies.

Stacked multi-cell (SMC) converter is one of the earliest hybrid multilevel topologies [15], [16]. It can be seen as the combination of two flying capacitor multilevel converters stacked together. Five-level active neutral-point clamped (5L-ANPC) converter is another hybrid multilevel topology which can be seen as the combination of a three-level ANPC and a two-level cell [17]–[19]. The main drawback of 5L-ANPC converter is the requirement of two switches connected in series to ensure all the switches withstand the same voltage stress, which may reduce the reliability of the converter.

In order to increase the voltage levels of three-level NPC and FC converters and overcome their inherent drawbacks, a four-level nested neutral-point clamped (4L-NNPC) converter derived from 3L-NPC topology is proposed in [20] and a four-level hybrid-clamped converter derived from 3L-FC topology is proposed in [21], [22]. However, all these hybrid topologies are the combination of NPC converters or FC converters and it is hard to output more than five voltage levels.

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Another kind of hybrid multilevel topology is the combination of CHB topology with other topologies, which can be divided into two types: asymmetrical hybrid multilevel topologies with unequal DC-link voltages [23]–[26], and symmetrical hybrid multilevel topologies with equal DC-link voltages [27]–[30]. Asymmetrical hybrid multilevel topologies achieve higher voltage level by adding or subtracting different DC-link voltages. Diverse DC-link voltage ratios have been studied in the literature to improve the output voltage levels [24]. One of the major issues of these topologies is the unequal power demands. In addition, the modularity is also lost.

Symmetrical hybrid multilevel topologies achieve higher output voltage level by using multilevel H-bridge cells. A five-level voltage can be obtained by using 3L-NPC or 3L-FC H-bridge and a nine-level voltage can be obtained by using 5L-ANPC H-bridge, as shown in Fig. 1.

In order to further increase the voltage levels of H-bridge cell and reduce the number of devices, the concept of using a multilevel DC-link (MLDCL) and an H-bridge to double the voltage levels is proposed in [27]. The MLDCL can be a NPC phase leg, a FC phase leg, or cascaded half-bridge cells. Based on this idea, a hybrid cascaded multilevel converter is studied in [28], as shown in Fig. 1(d). Cascaded half-bridge cells with isolated DC-sources are used as the MLDCL, which is suitable for battery energy storage system.

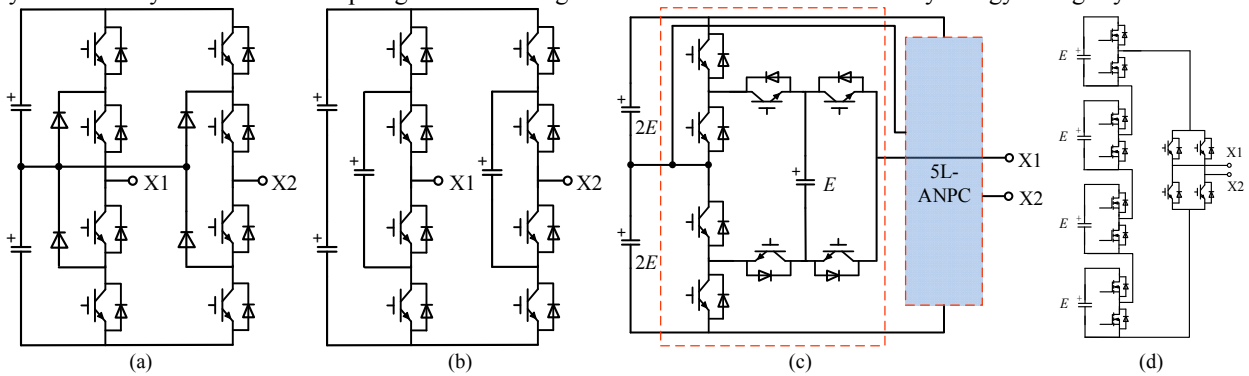

Fig. 1. Three multilevel H-bridge circuits: (a) 3L-NPC based 5L H-Bridge; (b) 3L-FC based 5L H-Bridge; (c) 5L-ANPC based 9L H-Bridge; (d) Hybrid cascaded nine-level converter.

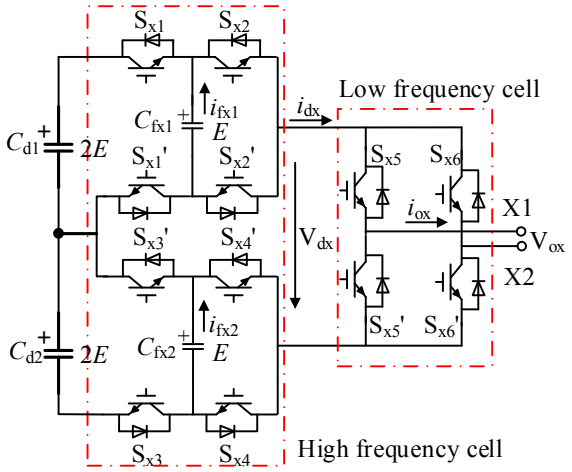

Fig. 2. The proposed nine-level H-bridge.

In order to reduce the number of isolated DC-sources, a symmetrical hybrid nine-level H-bridge cell is investigated in this paper, as shown in Fig. 2. Each phase of this converter is composed of a five-level DC/DC converter cell as MLDCL and an H-bridge cell. The DC/DC converter cell is operated at high frequency with low voltage devices and the H-bridge cell is operated at fundamental frequency with high voltage devices. Compared with the hybrid cascaded nine-level converter in Fig. 1(d), the number of isolated DC-sources is significantly reduced. Compared with 5L-ANPC H-bridge in Fig. 1(c), the main drawback of the proposed topology is that the low frequency switches in the H-bridge withstand the full DC-link voltage, while in 5L-ANPC it only bears half the DC-link voltage. However, the count of high voltage switches in the proposed topology is only half of that in the 5L-ANPC H-bridge topology. Moreover, the high voltage switches in the proposed topology are operated at zero-voltage switching, hence both the switching losses and turn-off surge voltage can be largely reduced.

A typical application of this topology is high speed motor drives. In some applications such as turbo compressors and blowers, high speed motors are utilized to improve the power density and can be connected to the load directly without gear boxes. In this situation the fundamental frequency can reach as high as several hundred to several kilo Hz, which means an extremely high switching frequency is required. This problem can be relieved by multilevel converters due to the high equivalent switching frequency, which is particularly suitable to apply hybrid multilevel converters.

For this symmetrical hybrid nine-level converter, there are two circuit configurations when used in motor drives. One configuration is that all the phase circuits are connected to a common DC-link and each drives an isolated winding of an open-winding motor, which is particularly suitable to drive a multi-phase motor with only one DC source, as shown in Fig. 3(a). Another configuration is that all the multilevel H-bridge cells are powered by isolated DC sources and can also be cascaded like traditional CHB converters, which is suitable

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for high voltage high speed Y-connected motors. Compared with traditional CHB converter, the symmetrical hybrid nine-level converter can reduce 3/4 of isolated DC sources when outputting the same voltage level. This paper is focused on the first configuration.

The key problem of this topology is the voltage balancing of DC-link capacitors and flying capacitors. This paper is a major revision of [31]. A detailed analysis of the average currents through the flying capacitor and neutral point of the DC-link is presented in this paper. A capacitor voltage balancing method based on phase-shifted PWM (PSPWM) is proposed. More simulation and experimental results are presented to demonstrate the feasibility of this topology and control method.

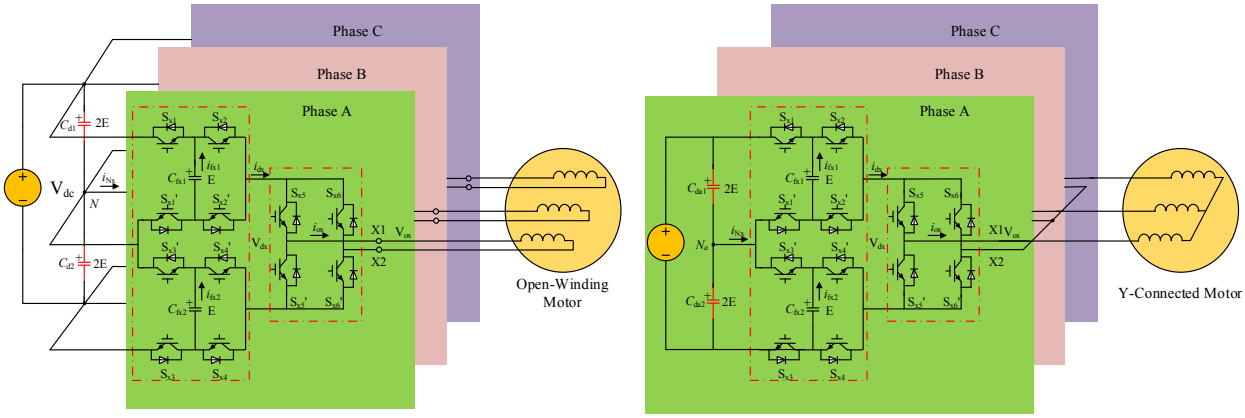

Fig. 3. Circuit diagram of the symmetrical hybrid nine-level inverter for motor drives: (a) for open-winding motor with a common DC-link; (b) for Y-connected motor with multiple isolated DC sources.

II. Operating Principles and Modulation Method

As shown in Fig. 2, the symmetrical hybrid nine-level inverter consists of two cells: a high frequency cell with low voltage devices and a low frequency cell with high voltage devices. The high frequency cell is composed of two three-level flying capacitor converters and the output voltage V_{dx} has five levels, which can be seen as a five-level DC/DC converter. For this five-level DC/DC converter, all the switches are operated at high frequency and the voltage ratings are only $V_{dc}/4$. The low frequency cell is an H-bridge and the voltage rating of four switches is V_{dc}. However, all the four switches are operated at fundamental frequency.

Assuming the DC-link voltage is constant and equal to $4E$, then the rated voltages of flying capacitor C_{fx1} and C_{fx2} are E. In order to output nine voltage levels, the following operating rules should be obeyed:

1) Switches S_{x1}–S_{x6} and S_{x1}'–S_{x6}' should be operated in a complementary way, respectively.
2) The H-bridge is operated with bipolar modulation. That is to say, S_{x5} and S_{x6}' are operated synchronously while S_{x6} and S_{x5}' are operated synchronously.

Based on the above operating rules, each phase can output 9 voltage levels with 32 distinct switching states. All the switching states are summarized in Table I. Different switching states have different effects on the flying capacitor voltages and neutral-point (NP) potentials, which provides a high degree of freedom to balance the voltages of DC-link capacitors and flying capacitors.

Defining the switching functions of switches S_{x1}–S_{x6} are S_{fx1}–S_{fx6}, respectively, based on Table I, the instantaneous output voltage of the high frequency cell can be written as:

$$V_{dx} = (S_{fx1} + S_{fx2} + S_{fx3} + S_{fx4}) \cdot E \tag{1}$$

Then the total output voltage can be written as:

$$V_{ox} = V_{dx} \cdot (S_{fx5} - S_{fx6}) \tag{2}$$

If E is selected as the base voltage value, then the range of V_{ox} is [–4, 4]. In order to operate S_{x5} and S_{x6} at fundamental frequency, S_{fx5} can be decided as follows:

$$S_{fx5} = \begin{cases} 0, & u_{ox} \le 0 \\ 1, & u_{ox} > 0 \end{cases}, \tag{3}$$

where u_{ox} is the reference output phase voltage. Then the reference modulation voltage u_{refx} for the high frequency cell can be written as follows:

$$u_{refx} = \begin{cases} u_{ox}, & S_{fx5} = 1 \\ -u_{ox}, & S_{fx5} = 0 \end{cases} \tag{4}$$

Equation (1) indicates that the output voltage of the low voltage cell is determined by the sum of the switching functions S_{fx1}–S_{fx4}. Moreover, switches S_{x1}, S_{x2}, S_{x3} and S_{x4} are independent of each other, so that classic phase-shifted PWM (PS-PWM) can be used to control the high frequency cell. Fig. 4 illustrates the diagram of the PS-PWM method applied in this five-level DC/DC converter cell. The four carrier signals are phase shifted by 90° and correspond to switches S_{x1}, S_{x2}, S_{x3} and S_{x4}, respectively. According to (1), a five-level DC voltage can be synthetized.

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TABLE I SWITCHING STATES OF THE SYMMETRICAL HYBRID NINE-LEVEL INVERTER

S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	switching states	V_{ox}
0	0	0	0	1	0	**V0**	**0**
0	0	0	1	1	0	**V1**	***E***
0	0	1	0	1	0	**V2**	***E***
0	1	0	0	1	0	**V3**	***E***
1	0	0	0	1	0	**V4**	***E***
0	0	1	1	1	0	**V5**	**2*E***
0	1	1	0	1	0	**V6**	**2*E***
1	1	0	0	1	0	**V7**	**2*E***
0	1	0	1	1	0	**V8**	**2*E***
1	0	1	0	1	0	**V9**	**2*E***
1	0	0	1	1	0	**V10**	**2*E***
0	1	1	1	1	0	**V11**	**3*E***
1	0	1	1	1	0	**V12**	**3*E***
1	1	0	1	1	0	**V13**	**3*E***
1	1	1	0	1	0	**V14**	**3*E***
1	1	1	1	1	0	**V15**	**4*E***
0	0	0	0	0	1	**V16**	**0**
0	0	0	1	0	1	**V17**	**–*E***
0	0	1	0	0	1	**V18**	**–*E***
0	1	0	0	0	1	**V19**	**–*E***
1	0	0	0	0	1	**V20**	**–*E***
0	0	1	1	0	1	**V21**	**–2*E***
0	1	1	0	0	1	**V22**	**–2*E***
1	1	0	0	0	1	**V23**	**–2*E***
0	1	0	1	0	1	**V24**	**–2*E***
1	0	1	0	0	1	**V25**	**–2*E***
1	0	0	1	0	1	**V26**	**–2*E***
0	1	1	1	0	1	**V27**	**–3*E***
1	0	1	1	0	1	**V28**	**–3*E***
1	1	0	1	0	1	**V29**	**–3*E***
1	1	1	0	0	1	**V30**	**–3*E***
1	1	1	1	0	1	**V31**	**–4*E***

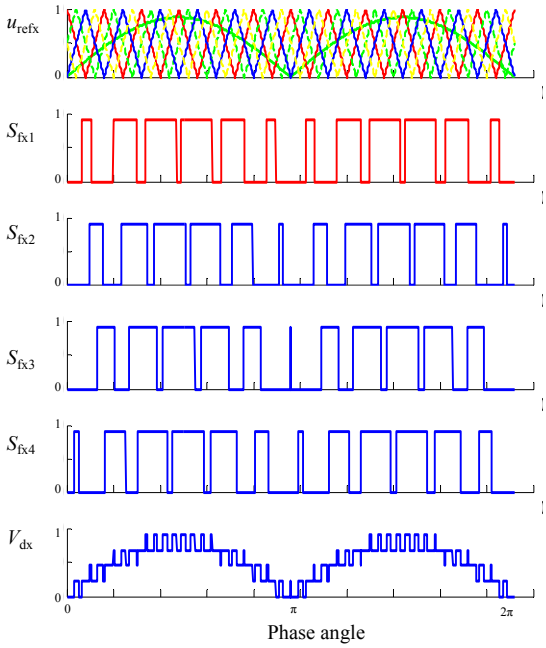

Fig. 4. Diagram of the PS-PWM. From top to button are: triangular carrier waves and reference wave, switching signal of S_{x1} to S_{x4}; synthetic five-level DC voltage.

III. CAPACITOR VOLTAGE BALANCING METHOD

A. Mathematical Model

One of the most important issues of this converter is the capacitor voltage balancing problem, including the voltage balancing of flying capacitors and DC-link capacitors. A mathematical model of the capacitor currents should be established first.

For the flying capacitors C_{fx1} and C_{fx2}, the instantaneous flying capacitor currents (i_{fx1}, i_{fx2}) can be written as:

$$\begin{cases} i_{fx1} = (S_{fx2} - S_{fx1}) \cdot i_{dx} \\ i_{fx2} = (S_{fx4} - S_{fx3}) \cdot i_{dx} \end{cases} \tag{5}$$

where i_{dx} is the current flows out of the high-frequency cell and can be written as follows:

$$i_{dx} = (S_{fx5} - S_{fx6}) \cdot i_{ox} \tag{6}$$

For the DC-link capacitors, the instantaneous NP currents i_{Nx} can be written as:

$$i_{Nx} = (1 - S_{fx1}) \cdot i_{dx} - (1 - S_{fx3}) \cdot i_{dx} = (S_{fx3} - S_{fx1}) \cdot i_{dx} \tag{7}$$

Defining the duty ratios of S_{fx1}–S_{fx4} are d_{x1}–d_{x4}, respectively, based on (1), the average output voltage of the low voltage cell in a carrier period can be written as:

$$u_{dx} = (d_{x1} + d_{x2} + d_{x3} + d_{x4}) \cdot E \tag{8}$$

If the carrier frequency is high enough, the reference signal can be regarded as a constant in a carrier period. Then the duty ratio of S_{fx1}–S_{fx4} in a carrier period can be written as:

$$d_{x1} = d_{x2} = d_{x3} = d_{x4} = u_{refx} / 4 \tag{9}$$

Based on (5), the average flying capacitor currents in a carrier period can be written as:

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$$\begin{cases} \bar{i}_{\mathrm{fx1}} = (d_{\mathrm{x2}} - d_{\mathrm{x1}}) \cdot i_{\mathrm{dx}} \\ \bar{i}_{\mathrm{fx2}} = (d_{\mathrm{x4}} - d_{\mathrm{x3}}) \cdot i_{\mathrm{dx}} \end{cases} \tag{10}$$

Based on (7), the average NP currents in a carrier period can be written as:

$$\bar{i}_{\mathrm{Nx}} = (d_{\mathrm{x3}} - d_{\mathrm{x1}}) \cdot i_{\mathrm{dx}} \tag{11}$$

From (9), (10) and (11) it can be seen that the average flying capacitor currents and NP current in a carrier period are zero, which indicates that the voltages across the flying capacitors and DC-link capacitors can be naturally balanced in a carrier period under ideal and steady-state conditions.

B. Capacitor voltage balancing method

Although the flying capacitor voltages and NP voltage can be naturally balanced under ideal and steady conditions, it also may diverge under non-ideal and dynamic conditions if not controlled. Define Δu_{fx1} and Δu_{fx2} are the voltage ripples of flying capacitors in a carrier period, which can be written as follows:

$$\begin{cases} \Delta u_{\mathrm{fx1}} = u_{\mathrm{fx1}} - E = -\dfrac{\bar{i}_{\mathrm{fx1}} \cdot T_{\mathrm{s}}}{C_{\mathrm{f}}} = \dfrac{T_{\mathrm{s}}}{C_{\mathrm{f}}}(d_{\mathrm{x1}} - d_{\mathrm{x2}}) \cdot i_{\mathrm{dx}} \\ \Delta u_{\mathrm{fx2}} = u_{\mathrm{fx2}} - E = -\dfrac{\bar{i}_{\mathrm{fx2}} \cdot T_{\mathrm{s}}}{C_{\mathrm{f}}} = \dfrac{T_{\mathrm{s}}}{C_{\mathrm{f}}}(d_{\mathrm{x3}} - d_{\mathrm{x4}}) \cdot i_{\mathrm{dx}} \end{cases} \tag{12}$$

where C_{f} is the capacitance of flying capacitors and T_{s} is the carrier period.

For the DC-link capacitor voltages, if the neutral points of three-phase circuits are connected together, the neutral-point voltage ripple is affected by the three-phase currents at the same time. Then the voltage ripple affected by a single phase can be written as follows:

$$\Delta u_{\mathrm{Nx}} = \frac{u_{\mathrm{d1}} - u_{\mathrm{d2}}}{2} = \frac{\bar{i}_{\mathrm{Nx}} \cdot T_{\mathrm{s}}}{2C_{\mathrm{d}}/3} = \frac{3T_{\mathrm{s}}}{2C_{\mathrm{d}}}(d_{\mathrm{x3}} - d_{\mathrm{x1}}) \cdot i_{\mathrm{dx}} \tag{13}$$

where C_{d} is the capacitance of upper and lower DC-link capacitors. From (12) and (13) it can be seen, a way to regulate the flying capacitor and NP voltages is to adjust the duty cycles of S_{fx1}–S_{fx4}, which varies the operation time of redundant switching states essentially. So the PS-PWM method should be modified slightly to achieve this goal.

The proposed voltage balancing of DC-link capacitors and flying capacitors can divided into the following three steps:

Step 1: For the flying capacitor C_{fx1}, if $sign(\Delta u_{\mathrm{fx1}} * i_{\mathrm{dx}}) > 0$, according to (12), the duty ratio of S_{fx1} should be decreased and the duty ratio of S_{fx2} should be increased. In order to not affect the output voltage and other capacitor currents, the modified duty ratios of S_{fx1}–S_{fx4} can be written as:

$$\begin{cases} d_{\mathrm{x1}}' = d_{\mathrm{x1}} - \dfrac{1}{4}\Delta d_{\mathrm{x21}} \\ d_{\mathrm{x2}}' = d_{\mathrm{x2}} + \dfrac{3}{4}\Delta d_{\mathrm{x21}} \\ d_{\mathrm{x3}}' = d_{\mathrm{x3}} - \dfrac{1}{4}\Delta d_{\mathrm{x21}} \\ d_{\mathrm{x4}}' = d_{\mathrm{x4}} - \dfrac{1}{4}\Delta d_{\mathrm{x21}} \end{cases} \tag{14}$$

Thus, the average charging current of the flying capacitor C_{fx1} is as follows:

$$\bar{i}_{\mathrm{fx1}} = (d_{\mathrm{x2}}' - d_{\mathrm{x1}}') \cdot i_{\mathrm{dx}} = \Delta d_{\mathrm{x21}} \cdot i_{\mathrm{dx}} \tag{15}$$

Step 2: For the flying capacitor C_{fx2}, if $sign(\Delta u_{\mathrm{fx2}} * i_{\mathrm{dx}}) > 0$, according to (12), the duty ratio of S_{fx3} should be decreased and the duty ratio of S_{fx4} should be increased. In order to not affect the output voltage and other capacitor currents, the modified duty ratios of S_{fx1}–S_{fx4} can be written as:

$$\begin{cases} d_{\mathrm{x1}}'' = d_{\mathrm{x1}}' - \dfrac{1}{4}\Delta d_{\mathrm{x43}} \\ d_{\mathrm{x2}}'' = d_{\mathrm{x2}}' - \dfrac{1}{4}\Delta d_{\mathrm{x43}} \\ d_{\mathrm{x3}}'' = d_{\mathrm{x3}}' - \dfrac{1}{4}\Delta d_{\mathrm{x43}} \\ d_{\mathrm{x4}}'' = d_{\mathrm{x4}}' + \dfrac{3}{4}\Delta d_{\mathrm{x43}} \end{cases} \tag{16}$$

Thus, the average charging current of the flying capacitor C_{fx2} is as follows:

$$\bar{i}_{\mathrm{fx2}} = (d_{\mathrm{x4}}'' - d_{\mathrm{x3}}'') \cdot i_{\mathrm{dx}} = \Delta d_{\mathrm{x43}} \cdot i_{\mathrm{dx}} \tag{17}$$

Step 3: For the neutral point voltage, if $sign(\Delta u_{\mathrm{Nx}} * i_{\mathrm{dx}}) > 0$, according to (13), the duty ratio of S_{fx3} should be decreased and the duty ratio of S_{fx1} should be increased. In order to not affect the output voltage and other capacitor currents, the modified duty ratios of S_{fx1}–S_{fx4} can be written as:

$$\begin{cases} d_{\mathrm{x1}}''' = d_{\mathrm{x1}}'' + \dfrac{1}{2}\Delta d_{\mathrm{x31}} \\ d_{\mathrm{x2}}''' = d_{\mathrm{x2}}'' + \dfrac{1}{2}\Delta d_{\mathrm{x31}} \\ d_{\mathrm{x3}}''' = d_{\mathrm{x3}}'' - \dfrac{1}{2}\Delta d_{\mathrm{x31}} \\ d_{\mathrm{x4}}''' = d_{\mathrm{x4}}'' - \dfrac{1}{2}\Delta d_{\mathrm{x31}} \end{cases} \tag{18}$$

Thus, the average NP current is as follows:

$$\bar{i}_{\mathrm{Nx}} = (d_{\mathrm{x3}}''' - d_{\mathrm{x1}}''') \cdot i_{\mathrm{dx}} = -\Delta d_{\mathrm{x31}} \cdot i_{\mathrm{dx}} \tag{19}$$

Based on (14), (16) and (18), the final duty ratio variations can be written as follows:

$$\begin{cases} \Delta d_{\mathrm{x1}} = -\dfrac{1}{4}\Delta d_{\mathrm{x21}} - \dfrac{1}{4}\Delta d_{\mathrm{x43}} + \dfrac{1}{2}\Delta d_{\mathrm{x31}} \\ \Delta d_{\mathrm{x2}} = \dfrac{3}{4}\Delta d_{\mathrm{x21}} - \dfrac{1}{4}\Delta d_{\mathrm{x43}} + \dfrac{1}{2}\Delta d_{\mathrm{x31}} \\ \Delta d_{\mathrm{x3}} = -\dfrac{1}{4}\Delta d_{\mathrm{x21}} - \dfrac{1}{4}\Delta d_{\mathrm{x43}} - \dfrac{1}{2}\Delta d_{\mathrm{x31}} \\ \Delta d_{\mathrm{x4}} = -\dfrac{1}{4}\Delta d_{\mathrm{x21}} + \dfrac{3}{4}\Delta d_{\mathrm{x43}} - \dfrac{1}{2}\Delta d_{\mathrm{x31}} \end{cases} \tag{25}$$

Δd_{x21}, Δd_{x43} and Δd_{x31} are very small and can be controlled by a PI regulator. The diagram of this voltage balancing control method is shown in Fig. 5. With this method, the DC-link and flying capacitor voltages can be well balanced.

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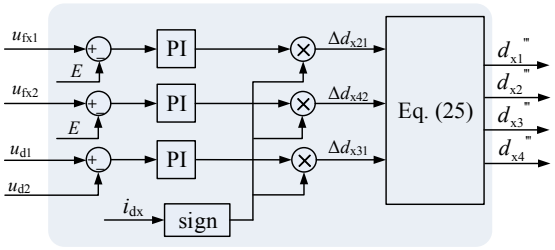


Fig. 5. Voltage balancing control diagram of the DC-link capacitors and flying capacitors

IV. Simulation Verification

In order to demonstrate the performance of the control method, a three-phase symmetrical hybrid nine-level inverter for a 3.3 kV/500 kVA high-speed open-winding motor is simulated in MATLAB/Simulink environment. The circuit structure is shown in Fig. 3(a).

In order to drive a 3.3kV open-winding motor, the DC-link voltage is set to 2800V. So the high voltage low frequency switches can use 4500 V IGBTs or IGCTs, which are operated at zero-voltage switching and the voltage stresses and power losses are very small. The flying capacitor voltage is set to 700 V and the switching frequency is set to 5 kHz. High speed 1200V IGBTs or SiC MOSFETs can be used as the low voltage high frequency switches. The fundamental frequency of the motor is 200Hz and the rated speed is 6000rpm. All the parameters used for simulation are summarized in Table II

TABLE II CIRCUIT PARAMETERS USED FOR SIMULATION

Parameters	Value
Rated volume	500 kVA
Rated line voltage	3.3 kV
DC-link voltage	U_{dc} = 2800 V
Flying capacitor voltage	E = 700V
DC-link capacitor	$C_{d1} = C_{d2}$ =200 μF
Flying capacitor	C_f = 200 μF
Carrier frequency	f_c = 5 kHz
Fundamental frequency	f_c = 200 Hz
Load	Open-winding induction motor

Fig. 6 shows the phase voltage and current waveforms of the motor starting process from 0 to 200Hz with variable voltage variable frequency (VVVF) control. The number of output phase voltage levels is increased from three to nine gradually. The detailed waveforms of steady states and FFT results are presented in Fig. 7. Due to the equivalent switching frequency of the output voltage is four times the carrier frequency, the main harmonics of the phase voltage are concentrated on carrier frequency (5 kHz) and four times the carrier frequency (20 kHz), as shown in Fig. 7, which are easy to filter out.

Fig. 8 and Fig. 9 are the DC-link capacitor voltages and flying capacitor voltages under the starting process. All the capacitor voltages are balanced at their nominal values, which demonstrates the effectiveness of the proposed voltage balancing method.

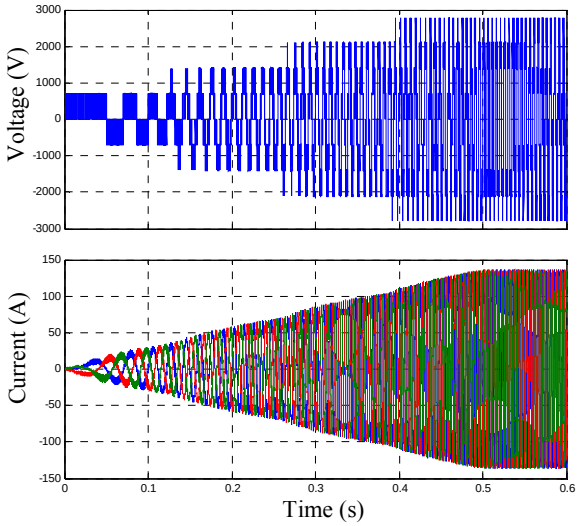
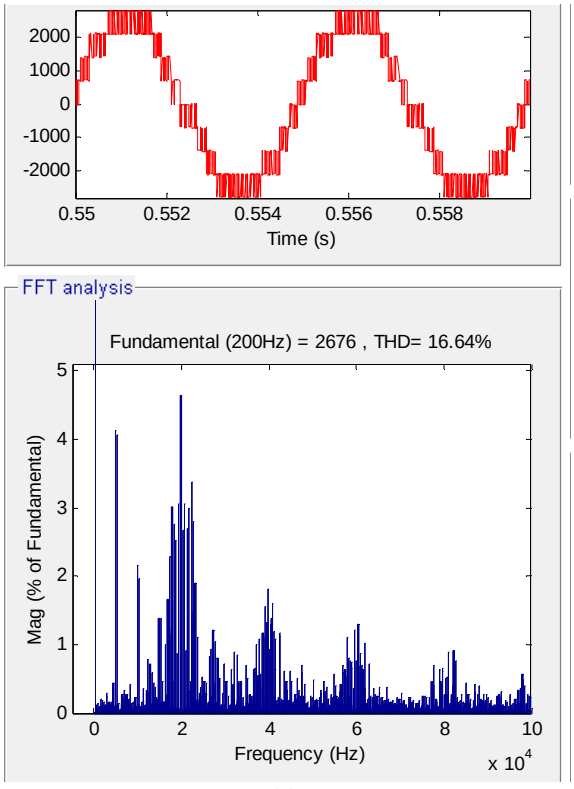


Fig. 6. Phase voltage and current of the motor starting from 0 to 200Hz.



(a)

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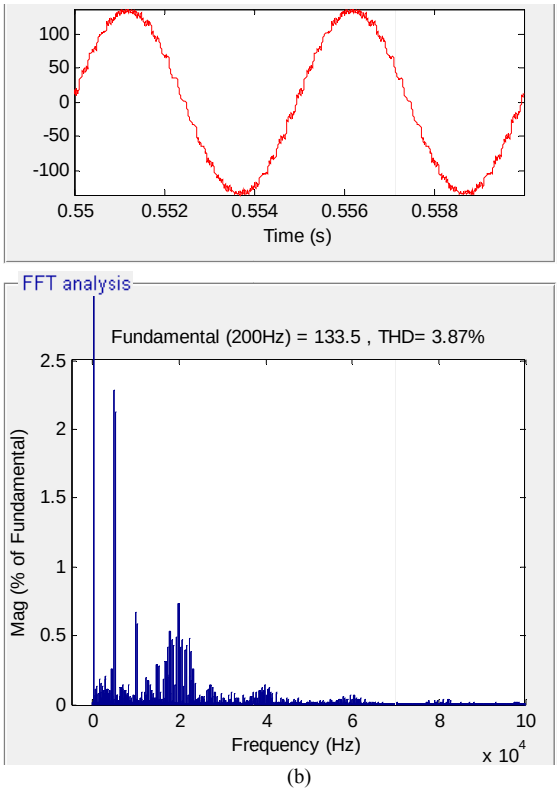

(b)

Fig. 7. The detailed phase voltage and current waveforms and FFT results: (a) phase voltage, (b) phase current

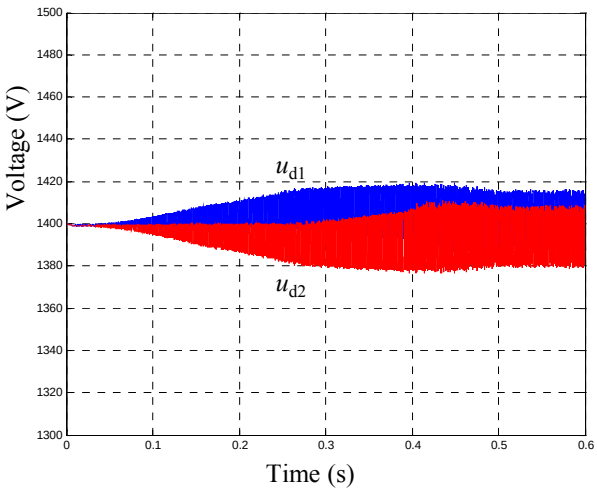

Fig. 8. The DC-link capacitor voltages during the motor start up process.

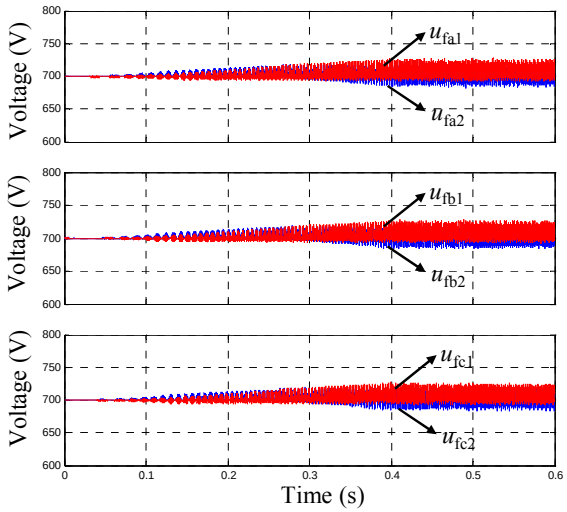

Fig. 9. The flying capacitor voltages during the motor start up process.

V. Experimental Verification

To verify the validity of the proposed voltage balancing method, a low power three-phase inverter prototype was built. A single phase circuit is shown in Fig. 10. The circuit parameters are shown in Table III. The low voltage switches used in the high frequency cell are MOSFETs IPB072N15N3 and the high voltage switches used in the low frequency cell are IGBTs IKB20N60T.

Fig. 10. A single phase circuit of the prototype

TABLE III Circuit parameters used for experiments

Parameters	Value
DC-link voltage	U_{dc} = 320 V
DC-link capacitor	$C_{d1} = C_{d2}$ = 2820 μF
Flying capacitor	C_f = 100 μF
Carrier frequency	f_c = 10 kHz
R-L Load	R = 22 Ω, L= 0.1 mH

Fig. 11 shows the experimental results of phase voltage and current with the modulation index m=1.0 and fundamental frequency f = 200Hz. A resistor-inductor (*R-L*) load is used at first. Fig. 12 shows the DC-link capacitor voltages and flying capacitor voltages of a single phase. It can be seen that all the capacitor voltages are balanced at their nominal values.

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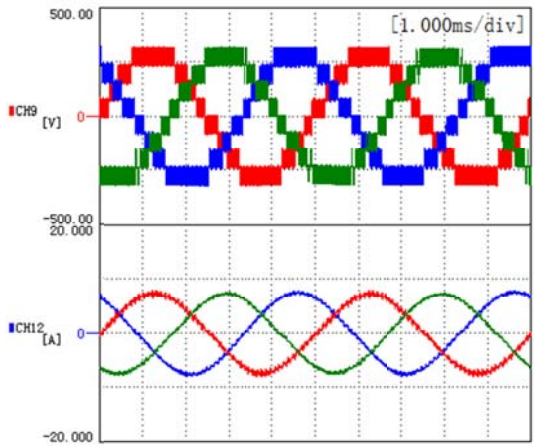

Fig. 11. Phase voltage (250V/div) and current (10A/div)

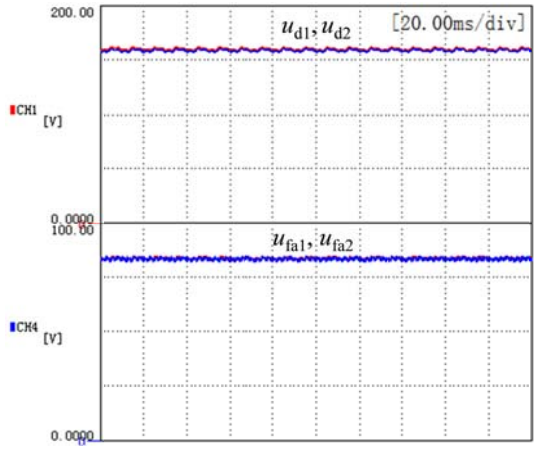

Fig. 12. The DC-link capacitor voltages (50V/div) and flying capacitor voltages (25V/div)

The FFT results of the phase voltage and current are presented in Fig. 13, which is realized by loading the experimental data into MATLAB and applying the same FFT analysis tool as the simulation. The main harmonics of the phase voltage are concentrated on carrier frequency (10 kHz) and four times the carrier frequency (40 kHz), which is similar with the simulation results.

Fig. 14 shows the dynamic performance of modulation index step change. The modulation index is stepped down from 1.0 to 0.2 and the number of phase voltage levels is decreased from nine to three. During the whole dynamic processes all the capacitor voltages remain balanced with the voltage balancing method.

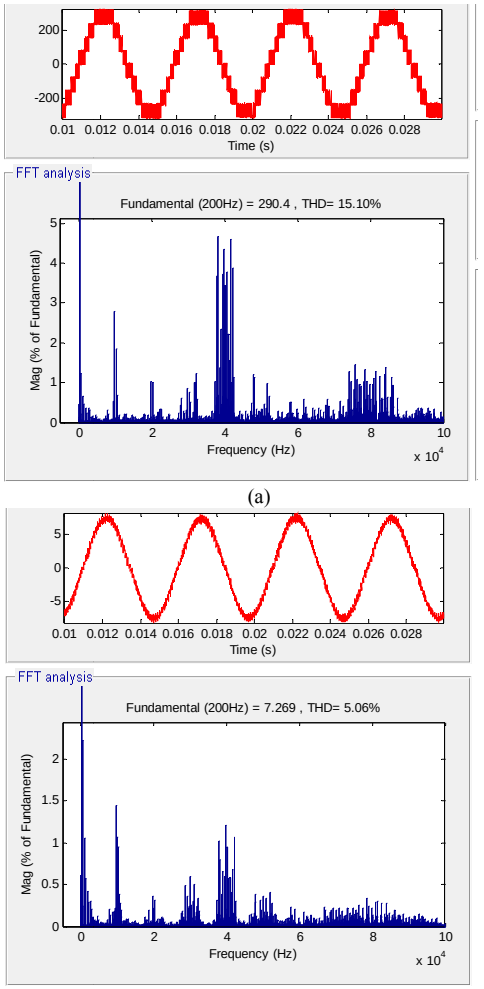

Fig. 13. The FFT results of (a) phase voltage and (b) phase current

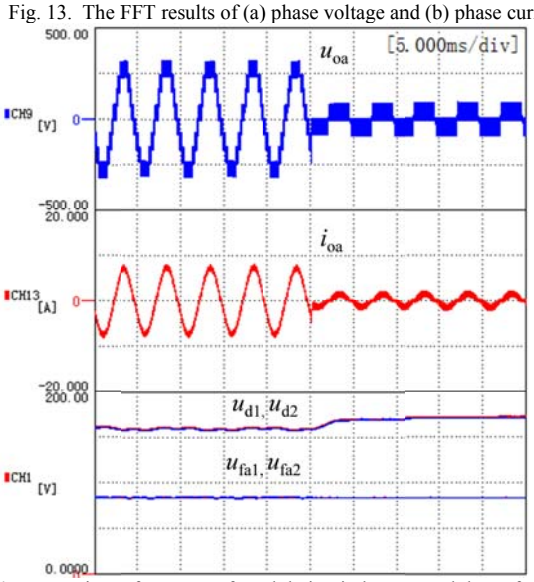

Fig. 14. Dynamic performance of modulation index stepped down from 1.0 to 0.2

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Fig. 15 and Fig. 16 show the experimental results of driving a three-phase open-winding induction motor. The motor is started up and accelerated from 0Hz to 50Hz in Fig. 15 and the flying capacitors are charged from zero to the nominal voltages with the voltage balancing method at the beginning. Fig .16 shows the performance of load torque step-change. During the whole accelerating and torque step-change processes, all the capacitor voltages maintain balanced. Steady and dynamic simulation and experimental results demonstrate the effectiveness of the capacitor voltage balancing method.

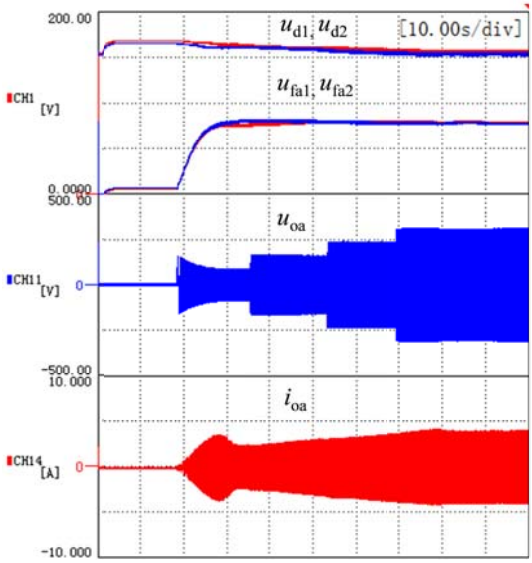

Fig. 15. Startup waveforms of an open-winding induction motor

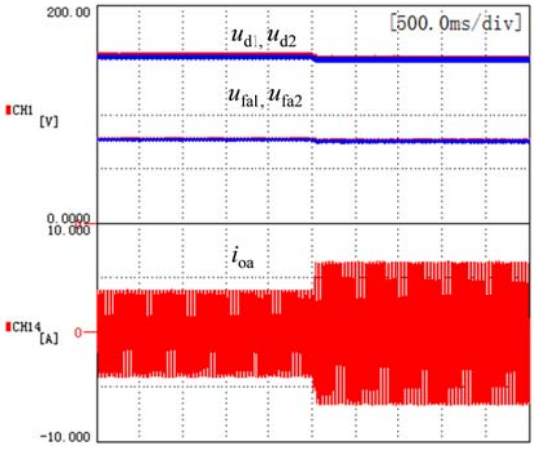

Fig. 16. Load torque step-change

VI. CONCLUSIONS

This paper introduced a symmetrical hybrid nine-level inverter for high speed motor drives. Each phase of this inverter is composed of a five-level DC/DC converter cell and an H-bridge cell. The five-level DC/DC converter cell is operated at high frequency with low voltage devices and the H-bridge cell is operated at fundamental frequency with high voltage devices. The operating principles and modulation method of this inverter is introduced and a capacitor voltage balancing method based on modified PS-PWM is proposed. Simulation and experimental results demonstrate the effectiveness of this voltage balancing method.

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