# A Series-Connected Three-Level Inverter Topology for Medium-Voltage Squirrel-Cage Motor Drive Applications

Suvajit Mukherjee and Gautam Poddar

***Abstract*—The application of pulsewidth-modulated (PWM) voltages using two-level high-voltage inverters to a squirrel-cage induction motor (SQIM) can cause heating of rotor shaft, voltage spike across the motor terminals, etc. The increase in the number of steps of the motor voltage and hence decreasing the $dv/dt$ applied to the machine terminals can be a solution to this problem. The existing topologies that generate this multistep voltage include cascading of a number of single-phase inverters or use of higher order multilevel inverters. In this paper, a topology with series connection of three-phase three-level inverters is proposed, which addresses the problems of medium-voltage drives. The design of the inverter topology and its various PWM techniques are presented in this paper. This inverter topology and its control are verified on a 7.5-hp SQIM drive. Experimental results validate the steady-state and dynamic performances of the drive.**

***Index Terms*—Medium-voltage ac drives, multilevel converter topologies.**

## NOMENCLATURE

| | |
|---|---|
| $L_s$, $L_r$ | Stator and rotor self-inductances referred to the stator. |
| $L_0$ | Magnetizing inductance. |
| $\sigma_s$, $\sigma_r$ | Stator and rotor leakage factors. |
| $\sigma$ | Total leakage factor. |
| $R_s$, $R_r$ | Stator and rotor resistances referred to stator. |
| $P$ | Number of poles of the motor. |
| $V_{sd}$, $V_{sq}$ | $d$- and $q$-axis stator voltages. |
| $V_{rd}$, $V_{rq}$ | $d$- and $q$-axis rotor voltages. |
| $\varepsilon$ | Angle between stator and rotor axes. |
| $\rho_{mr}$, $\rho_r$ | Rotor flux angle with respect to stator and rotor axes. |
| $\vec{\psi}_{rs\alpha}$, $\vec{\psi}_{rs\beta}$ | $\alpha$–$\beta$-axis rotor flux in stationary reference frame. |

## I. INTRODUCTION

IN A NORMAL squirrel-cage induction-motor (SQIM) drive, the motor is normally fed with pulsewidth-modulated (PWM) voltages which cause steep voltage wave fronts $(dv/dt)$ to appear across the motor terminals. This may lead to the motor insulation failure. In addition, motor damages are reported due to the high-voltage change rates $(dv/dt)$ which produces common-mode voltages across the motor windings [3]. High-frequency switching increases the gravity of this problem due to the increased number of times this common-mode voltage is applied in each cycle [1]–[4]. This is a matter of big concern for variable-speed medium-voltage drives where the voltage levels are very high. The above problem can be resolved by applying variable voltage with low $dv/dt$, i.e., by the use of multilevel inverter. By increasing the number of steps of the motor voltage as in multicell technologies [6], [7], the gravity of this problem can be reduced. Moreover, the multilevel inverters can effectively work at lower switching frequencies as compared to conventional PWM inverters [5], [6]. The proposed topology of series-connected three-level inverters increases the number of steps in the applied voltage and hence decreasing the $dv/dt$ applied to the machine terminals (i.e., terminal-voltage spike is reduced).

Similar voltage profiles can also be obtained by using higher order neutral-point-clamped (NPC) multilevel inverters [8], [9] or by cascading a number of two-level inverters [6], [7]. However, the multilevel NPC inverters suffer from dc-bus imbalance [18]–[20], device underutilization problems and unequal ratings of the clamped diodes [9], [10], etc., which are not very serious problems for inverters with three levels or lower. The capacitor voltage imbalance for a five-level one is presented in [18]–[20] which suggest the need of extra hardware in the form of dc choppers or a back-to-back connection of multilevel converters. The cascaded H-bridge topology [6]–[8] suffers from the drawbacks of the usage of huge dc-bus capacitors and complex input transformers for isolated dc bus for each module. These drawbacks are addressed in the proposed topology. Furthermore, the power circuit is modular in structure, and hence, the number of modules to be connected in series depends on the power of the drive.

In this paper, the proposed topology and its various PWM control strategies are experimentally validated on a vector-controlled SQIM drive [15]–[17]. It has two three-level inverters connected in series and drives the motor.

## II. POWER-CONVERTER TOPOLOGY

The proposed general configuration of "$n$" number of three-level inverters connected in series is shown in Fig. 1. Each

Paper 2009-IDC-078.R1, presented at the 2008 Industry Applications Society Annual Meeting, Edmonton, AB, Canada, October 5–9, and approved for publication in the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS by the Industrial Drives Committee of the IEEE Industry Applications Society. Manuscript submitted for review April 13, 2009 and released for publication July 7, 2009. First published November 17, 2009; current version published January 20, 2010.

S. Mukherjee is with the Research and Development Center, Emerson Network Power India Private, Ltd., Thane 400 602, India (e-mail: m_suvajit@yahoo.com).

G. Poddar is with the Department of Electrical Engineering, Indian Institute of Technology, Kharagpur 721 302, India (e-mail: gpoddar@ee.iitkgp.ernet.in).

Digital Object Identifier 10.1109/TIA.2009.2036283

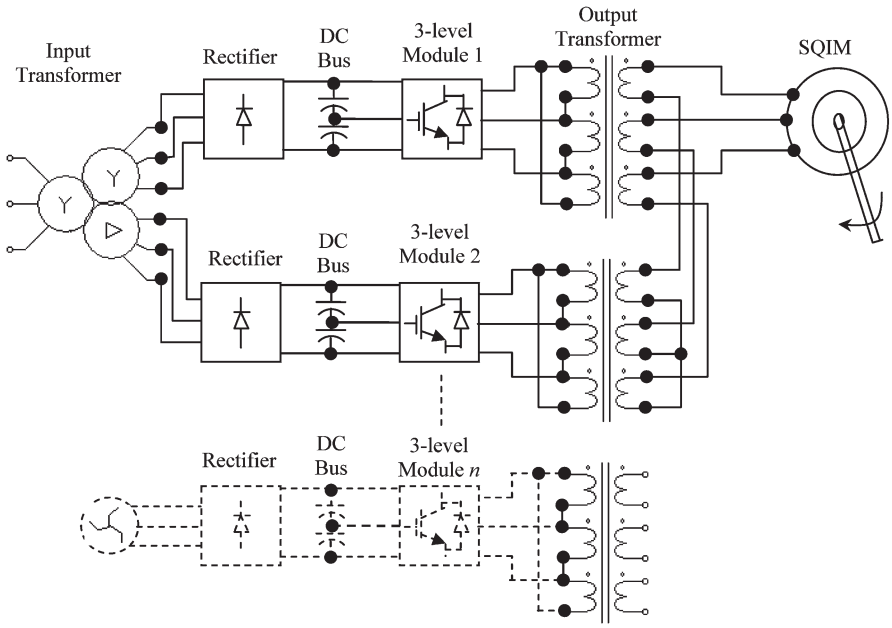



Fig. 1. Block diagram of three-phase three-level inverter modules connected in series driving an SQIM.

inverter module is a three-phase NPC three-level inverter. At the output stage, transformers are used to have the series connection of three-level inverters, as shown in Fig. 1. If "$V_{\rm dc}$" is the dc-bus voltage of each inverter module, then "$\alpha$" is the turns ratio of each transformer and "$n$" is the number of inverter modules then for sine PWM (SPWM) strategy; the motor rms phase voltage $(V_{\rm Ph\_motor})$ can be expressed as follows:

$$\text{rms of } V_{\rm Ph\_motor} = \sqrt{3}\alpha m n \frac{V_{\rm dc}}{2\sqrt{2}} \tag{1}$$

where $m$ is the modulation index of the inverter topology defined as follows:

$$m = \frac{\text{peak of } V_{\rm ph\_inverter}}{n\frac{V_{\rm dc}}{2}}. \tag{2}$$

$V_{\rm ph\_inverter}$ is the total phase voltage reference of the inverter topology. For the given peak of $V_{\rm Ph\_motor}$, peak of $V_{\rm ph\_inverter}$ can be computed as follows:

$$\text{peak of } V_{\rm ph\_inverter} = \frac{\text{peak of } V_{\rm ph\_motor}}{\sqrt{3}\alpha}. \tag{3}$$

The generation of individual reference voltage signal of each inverter is discussed as follows.

The gate pulses for each three-level inverter module can be derived using two carrier signals. Thus, "$n$" numbers of such three-level inverter modules require "$2n$" number of carriers [10], [13]. The three-phase voltage reference signals are then compared with these carrier waves to produce the gate pulses for the inverters. For example, the carrier waves and the sinusoidal modulating voltage signal (SPWM technique) for $R$ phase is shown in Fig. 2 for four series-connected three-level inverters. The carrier waves 1 and 1′ (Fig. 2) with $R$-phase voltage reference controls the inverter module 1. Similarly, 2–2′, 3–3′, and 4–4′ carrier waves with $R$-phase voltage reference

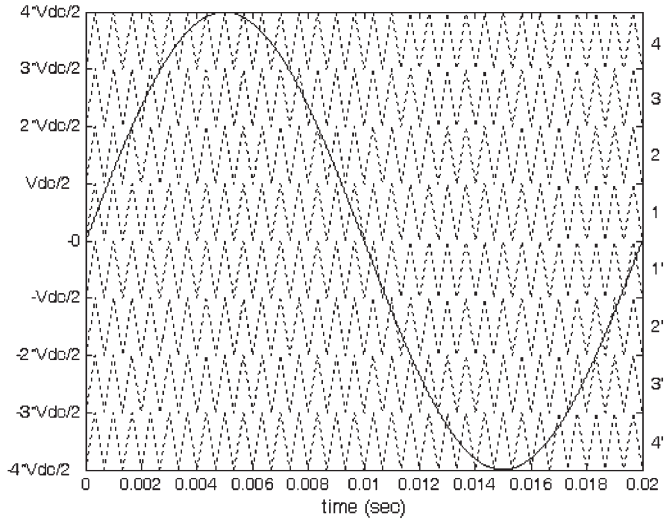



Fig. 2. Carrier waves and the sinusoidal modulating voltage signal for $R$ phase in SPWM technique.

generate the gate pulses for the three-level inverter modules 2, 3, and 4, respectively. Thus, each inverter module produces the voltage proportional to a part of the reference phase voltage signals. It is important to note that no two three-level inverter modules switch simultaneously (Fig. 2). Thus, the maximum $dv/dt$ rate of the output voltage of this topology is limited to that of a single three-level inverter module (Fig. 5). The references of each inverter are shown in Fig. 3. The corresponding output line voltages of each inverter are shown in Fig. 4. The four windings, one from each transformer, are connected in series and produced the net $R$-phase voltage, as shown in Fig. 5. Similarly, the other two phase voltages are generated.

The line voltage spectra of individual inverters are shown in Fig. 4 for switching frequency of 2.5 kHz. These line voltages get added to produce the net phase voltage of the topology. The voltage spectra are expressed as a percentage of the

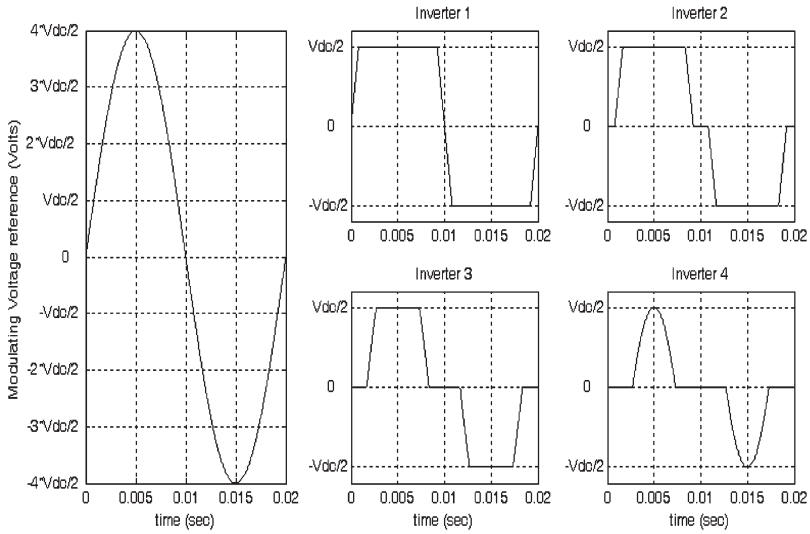



Fig. 3. Generation of modulating voltage signal for $R$ phase of each of the four inverters in series for SPWM strategy.

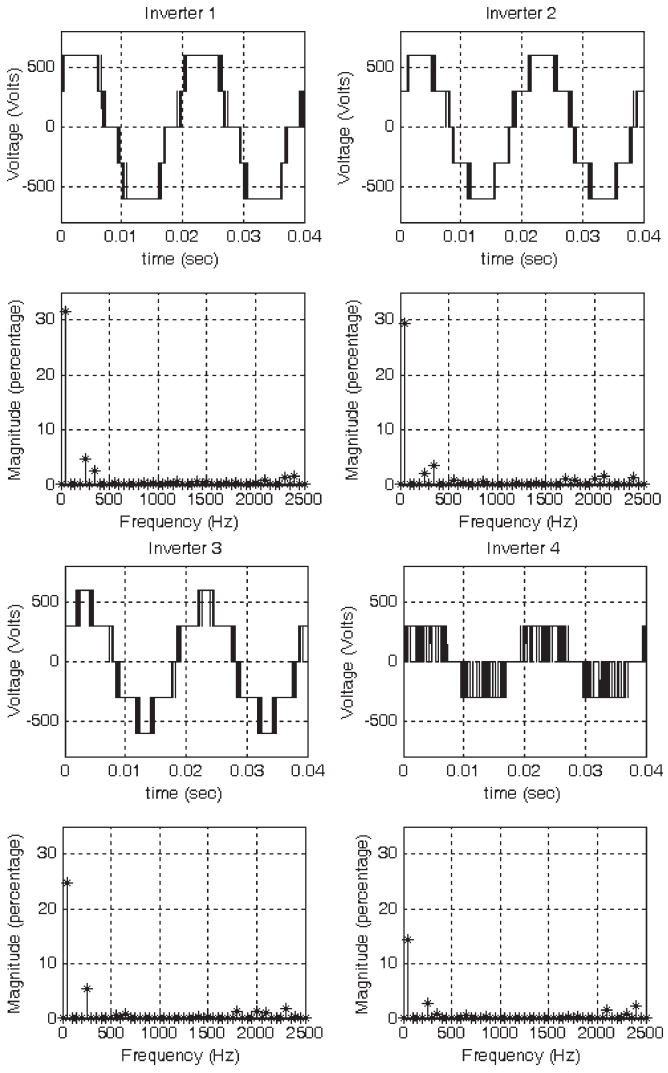



Fig. 4. Simulated line voltage and harmonic spectrum of inverters 1, 2, 3, and 4 when four inverters are connected in series with SPWM technique for $V_{\rm dc} = 600$ V, $\alpha = 1$, and $m = 1$.

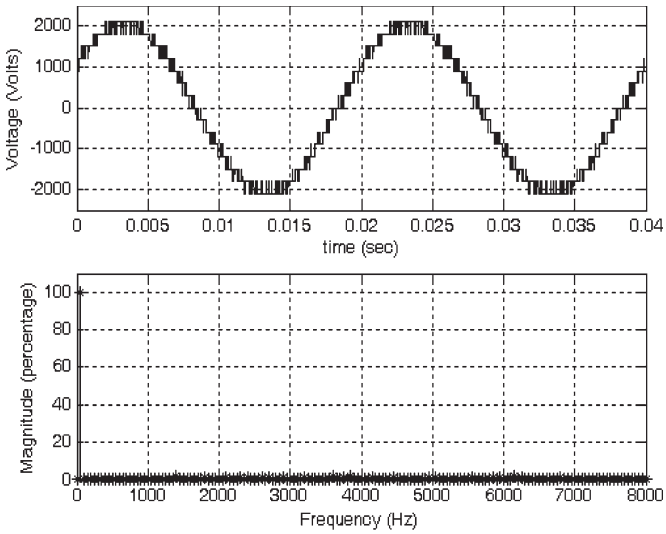



Fig. 5. Simulated phase voltage when four inverters are connected in series with SPWM technique for $f_{sw} = 2.5$ kHz, $V_{\rm dc} = 600$ V, $\alpha = 1$, and $m = 1$.

maximum total fundamental $(V_{\rm peak})$ that can be produced by the topology

$$V_{\rm peak} = \sqrt{2} * V_{\rm Ph\_motor} \tag{4}$$

or $V_{\rm peak} = 2078.5$ V for $V_{\rm dc} = 600$ V, $n = 4$, $\alpha = 1$, and $m = 1$ using (1). Hence, the spectra show the percentage share of the fundamental of each inverter module. These spectra also suggest that the line voltages of all these inverters contain additional small amount of the 5th-, 7th-, 11th-, 13th-, and higher order harmonics besides the normal switching harmonics. However, the net phase voltage and line voltage of this topology do not contain any of these harmonics, as suggested by the spectra shown in Fig. 5. These harmonics get canceled when the line voltages of the individual inverters are added by the transformers to produce the net phase voltages. The increased number of steps in the motor terminal voltage reduces the $dv/dt$ as that compared with a conventional two-level inverter.

## III. Design of Inverter Modules

The general configuration of a sensorless SQIM drive with "$n$" number of three-phase voltage source modules connected in series is shown in Fig. 1. Each voltage source module consists of a three-phase diode rectifier, a dc bus, a three-phase three-level NPC inverter, and a three-phase transformer. In this section, design guidelines are presented for each module to drive a motor of voltage and current ratings $V_s$ and $I_s$, respectively.

### A. Design of Transformer and Inverter for Each Module

The primary side of each three-phase transformer is chosen as delta connected while the secondary side is kept open for the series connection between the modules. Normally, the dc-bus voltage $(V_{\rm dc})$ of each module is chosen such that the standard insulated-gate bipolar transistor (IGBT) module (for example, 1400-V IGBT, 300 A) can be used. Similarly, the current rating $(I_{\rm inv})$ of each inverter module is chosen. Now, the current required on the motor side of the transformer is $I_s$. Then, the current drawn from the inverter is $I_s * \alpha * \sqrt{3}$ and must be equal to $I_{\rm inv}$. In this paper, $\alpha$ is the transformer turns ratio defined as follows:

$$\alpha = \frac{\text{number of transformer phase turns on the motor side}}{\text{number of transformer phase turns on the inverter side}}. \tag{5}$$

Thus, the turns ratio of the transformer $(\alpha)$ is obtained as follows:

$$\alpha = \frac{I_{\rm inv}}{\sqrt{3} * I_s}. \tag{6}$$

For $n$ number of modules, the maximum line voltage, which this topology can produce, is $\sqrt{3} * V_{\rm dc}(\alpha * n/\sqrt{2})$, assuming space-vector PWM (SVPWM) strategy. This voltage must match the required motor line voltage $V_s$. Thus, the number of modules $n$ can be selected as follows:

$$n = \frac{\sqrt{2} * V_s}{\sqrt{3} * \alpha * V_{\rm dc}} = \frac{\sqrt{2} * V_s * I_s}{V_{\rm dc} * I_{\rm inv}}. \tag{7}$$

At maximum modulation index in the linear modulation zone, all the modules share the net fundamental output voltages almost equally. In addition, all the modules also have some amount of fifth-, seventh-, and higher order voltage harmonics besides the very small amount of switching harmonics. These voltage harmonics must be taken care of while designing the standard transformer for each module. However, all the module currents, and hence the transformer currents, remain almost sinusoidal.

### B. Selection of DC-Bus Capacitor for Each Module

In single-phase inverters, the dc bus carries second-harmonic currents in addition to the switching currents. Therefore, the size of the capacitors increases when single-phase inverters are used in cascaded H-bridge topology [6]. Since the proposed drive has three-phase inverter at the output stage, the low-frequency (second harmonic) ripple in the capacitor will not be present. Therefore, the size of the capacitor will be relatively small in the case of the proposed topology.

If any module fails, the inverter output of the faulty module can be bypassed (by a switch), and the topology can operate with reduced output voltage and hence reduced power. Therefore, for one module failure among "$n$" number of series-connected module, the output voltage will decrease to "$n-1/n$" times although the same output current can be delivered. Hence, the power rating of the drive will decrease to "$n-1/n$" times.

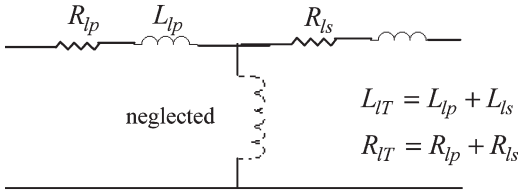



Fig. 6. Equivalent circuit of a single-phase transformer with 1:1 turns ratio.

## IV. SQIM Drive Using Proposed Converter

The general configuration of a sensorless SQIM drive with "$n$" number of NPC three-level inverter is shown in Fig. 1. All three-level inverters, connected in series, drive the motor and share the load.

### A. Rotor-Flux-Oriented SQIM

In this topology, the stator leakage inductance value has to be modified to incorporate the leakage inductance of the output transformers $(L_{lT})$. In addition, the effective stator resistance changes due to the presence of transformer winding resistances $(R_{lT})$. By neglecting the magnetizing branch of the inverter transformer, the equivalent circuit of the transformer is a simple $R$–$L$ circuit, as shown in Fig. 6. Thus, the modified values of the stator leakages are as follows:

$$\begin{aligned} \sigma L_s' &= \sigma L_s + L_{lT} \\ R_s' &= R_s + R_{lT}. \end{aligned} \tag{8}$$

Hence, the modified dynamical equations of the SQIM voltages and currents in the $d$–$q$ plane are presented as follows:

$$V_{sd} = R_s' i_{sd} + \sigma L_s' \frac{di_{sd}}{dt} - \underline{\sigma L_s' \omega_{mr} i_{sq}} + \underline{\frac{1}{(1+\sigma_r)} \frac{d\psi_r}{dt}} \tag{9}$$

$$V_{sq} = R_s' i_{sq} + \sigma L_s' \frac{di_{sq}}{dt} + \underline{\sigma L_s' \omega_{mr} i_{sd}} + \underline{\frac{\psi_r \omega_{mr}}{(1+\sigma_r)}} \tag{10}$$

where the $d$-axis is aligned with the rotor flux vector $(\vec{\psi}_r)$[17], [21]. The rotor flux vector in stationary coordinates $(\vec{\psi}_{rs})$ is expressed in terms of stator flux as

$$\vec{\psi}_{rs} = \frac{L_r}{L_0}\{\vec{\psi}_s - \sigma L_s \vec{i}_s\}. \tag{11}$$

The stator flux $\vec{\psi}_s$ is estimated from the stator voltage $\vec{V}_s$ as follows:

$$\vec{\psi}_s = \int (\vec{V}_s - R_s \vec{i}_s - \omega_c \vec{\psi}_s). \tag{12}$$

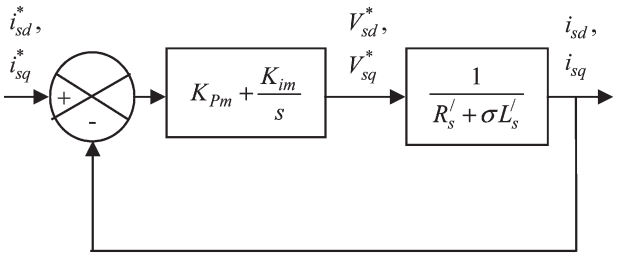



Fig. 7. $d$- and $q$-axis motor current controller.

The problem integration at low frequency is tackled by replacing the pure integration of stator voltage with a low-pass filter (cutoff frequency $= \omega_c$) [15], [17].

### B. Motor Controller

The $d$- and the $q$-axis motor-voltage equations (9) and (10) show the first-order dynamics of the stator currents ($i_{sd}$ and $i_{sq}$) if the underlined terms are decoupled. Therefore, simple PI controllers with unity feedback system can control the $d$–$q$-axis motor currents to control the flux and the torque of the motor, as shown in Fig. 7. By choosing the proper gain values of the PI controllers, the desired bandwidth $(1/\tau_{im})$ of the motor current controller is achieved [17]. Thus, the closed-loop transfer functions of $i_{sd}$ and $i_{sq}$ become as follows:

$$\frac{i_{sd}(s)}{i_{sd}^*(s)} = \frac{1}{1 + s\tau_{im}}$$
$$\frac{i_{sq}(s)}{i_{sq}^*(s)} = \frac{1}{1 + s\tau_{im}}. \quad (13)$$

In this paper, the desired response time $\tau_{im}$ of the motor current is chosen as 4 ms. Finally, the outputs of the PI controllers are added to the underlined coupling terms of (9) and (10) to get the actual $d$- and $q$-axis voltage references $(V_{sd}^*, V_{sq}^*)$ [17].

It is important to note that the motor phase voltages and the inverter phase voltages are not in phase. The motor phase voltage is in phase with the line voltages of the inverter modules. Hence, a phase shift of 30° is provided to the three motor phase voltage references obtained to generate the three inverter phase voltage references. The phase reference obtained is the total phase reference of the topology. Hence, this reference is obtained by adding the reference of the individual inverter modules.

The input transformer with a delta and wye secondary for two three-level modules is shown in Fig. 1. If more number of modules is used, then the same secondary delta and wye can be loaded with parallel connections as an isolated dc bus is not required. This is in contrast to the cascaded H-bridge topology, which requires an isolated dc bus for each module. However, if the input current needs to be shaped, the input transformer with zigzag secondary can be used.

## V. Experimental Results

The experimental verification is carried out on a 7.5-hp SQIM. The inverters used for this drive are three-phase 5-kVA three-level diode-clamped inverters. Two inverters are used to demonstrate the control strategy, as discussed earlier. The

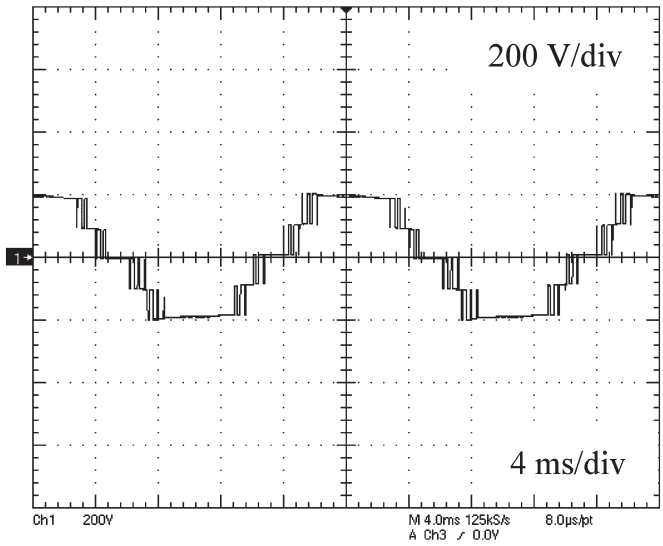



Fig. 8. Experimental waveform of steady-state inverter 1 line voltage.

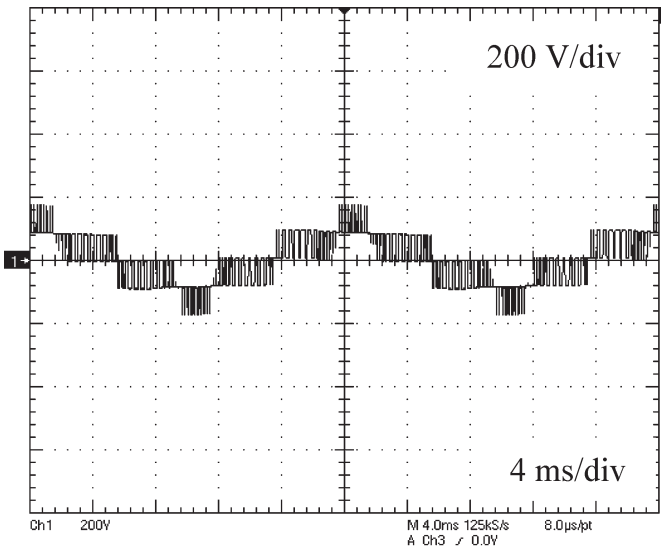



Fig. 9. Experimental waveform of steady-state inverter 2 line voltage.

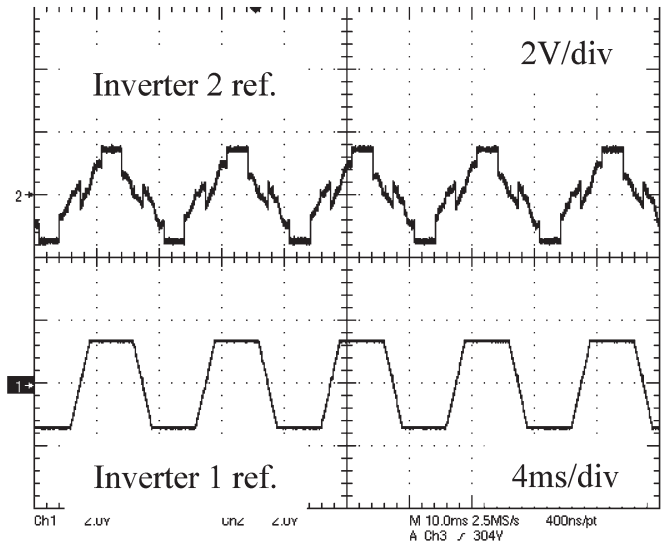
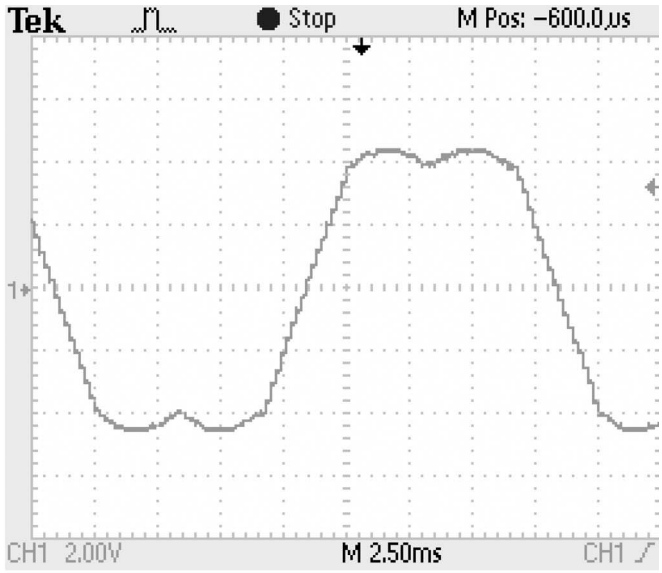
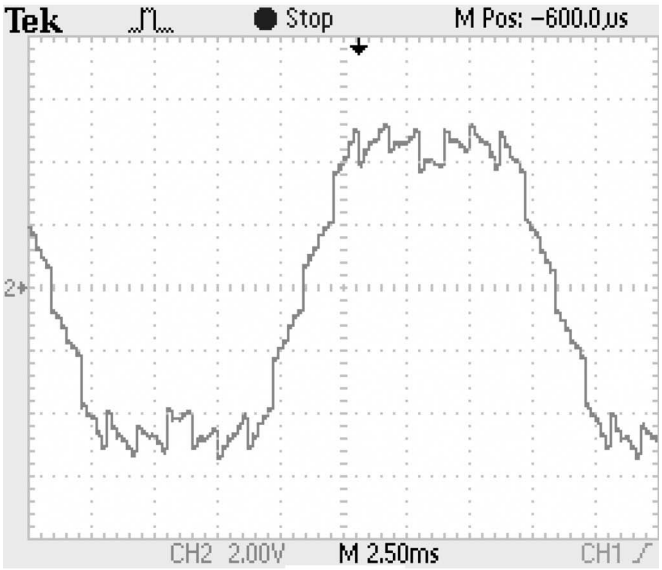



Fig. 10. Experimental waveform of inverter references in bus clamp technique.

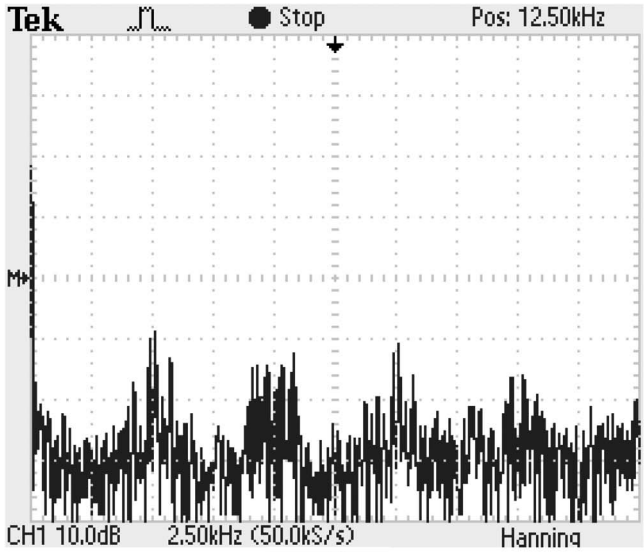



(a)

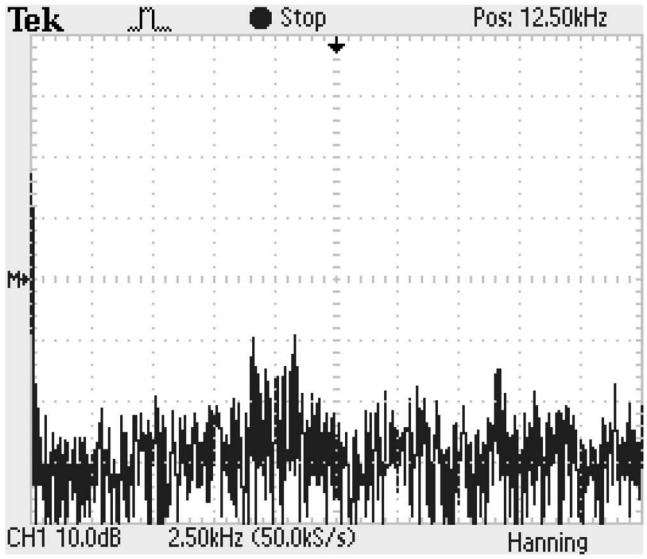



(b)

Fig. 11. Experimental waveform of inverter reference with (a) carrier-based PWM with third-harmonic injection technique; (b) CSVPWM technique.




(a)




(b)

Fig. 12. Experimental waveform of the harmonic analysis of the motor phase voltage obtained with (a) carrier-based PWM with third-harmonic injection technique; (b) CSVPWM technique ($f_{sw} = 5$ kHz).

switching frequency of the individual inverter is 5 kHz. The complete control strategy is implemented on a digital controller.

Figs. 8 and 9 show the individual inverter line voltages that are being added up. This suggests that each inverter has low-voltage steps (low $dv/dt$) that are being added up to produce the final terminal voltage across the motor. The switching in the inverters is also less as compared to conventional PWM inverters.

Various types of PWM techniques (apart from SPWM) are used for the generation of the reference wave of each inverter. The voltage references for individual converters in bus clamp technique are shown in Fig. 10. This technique provides reduced switching and hence decreases the switching loss of the inverter [11], [12]. Fig. 11 shows the inverter phase voltage references with carrier-based PWM with third-harmonic injection technique and also with centered SVPWM technique (CSVPWM) [13]. The harmonic profile in the CSVPWM technique is optimized by the judicious usage of the duty cycles of the voltage vectors during each switching period [13], [14]. Fig. 12 shows the harmonic spectra of the motor phase voltage obtained with various PWM techniques whose references are shown in Fig. 11. The spectra reveal that the CSVPWM technique produces dominating harmonics starting near the double switching frequency (10 kHz), while the PWM technique with third-harmonic injection produces dominating harmonics starting near the switching frequency (5 kHz). Thus, CSVPWM technique causes less motor flux and current ripple as the dominant harmonic components of the applied motor voltage lie at relatively higher frequency.

The phase voltage waveform along with its spectrum analysis is shown in Fig. 13. It confirms stepped voltage waveform and low $dv/dt$ that are applied to the motor. Hence, due to the low $dv/dt$ in the terminal voltage applied to the motor, the stress in the motor windings are reduced. Fig. 14 shows the

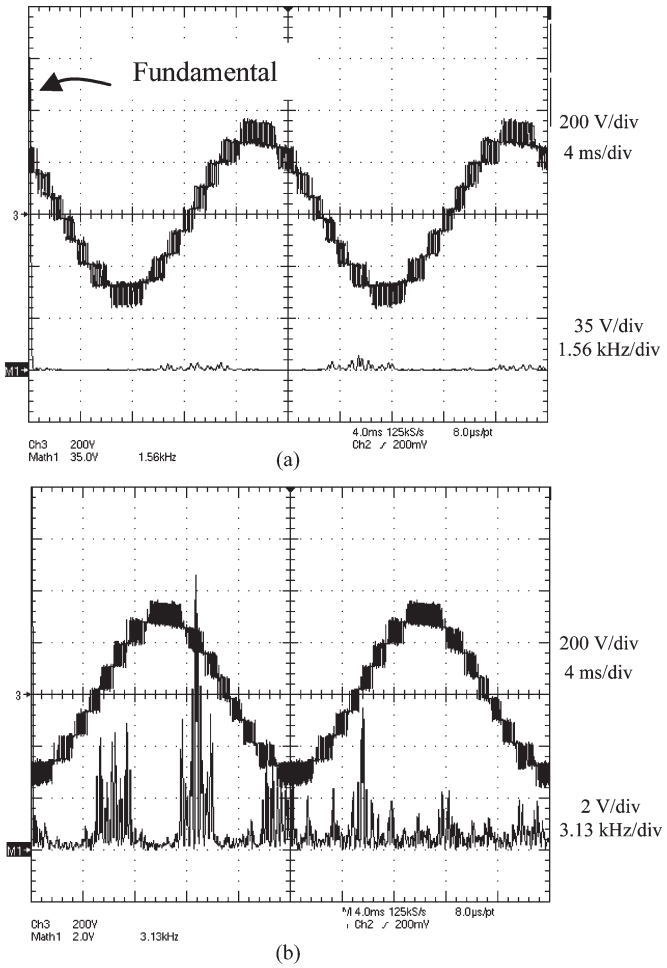



Fig. 13. (a) Experimental waveform of steady-state motor phase voltage $(V_{s1})$ and its spectral analysis showing the relative magnitude of fundamental and harmonics; (b) zoomed harmonic spectrum $(f_{sw} = 5$ kHz).

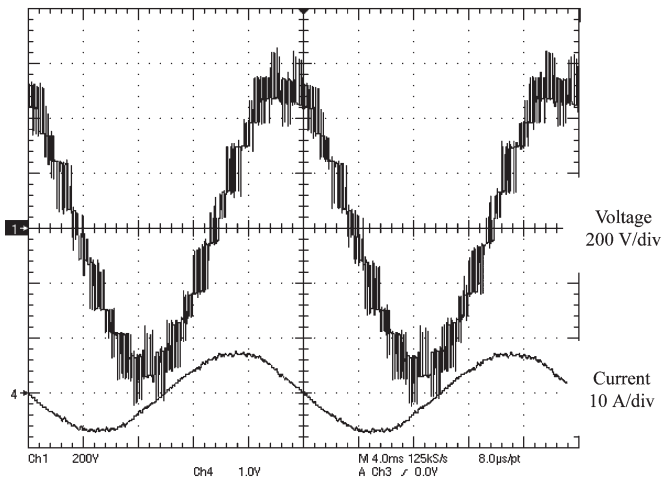



Fig. 14. Experimental waveform of steady-state motor current $(i_{s1})$ and motor line voltage.

steady-state motor line voltage and motor current. Fig. 15 shows the variation of motor phase voltage and motor speed for a step change in torque command. It shows smooth speed transient of the drive without much voltage spikes during the transient. Hence, the motor windings are not much stressed

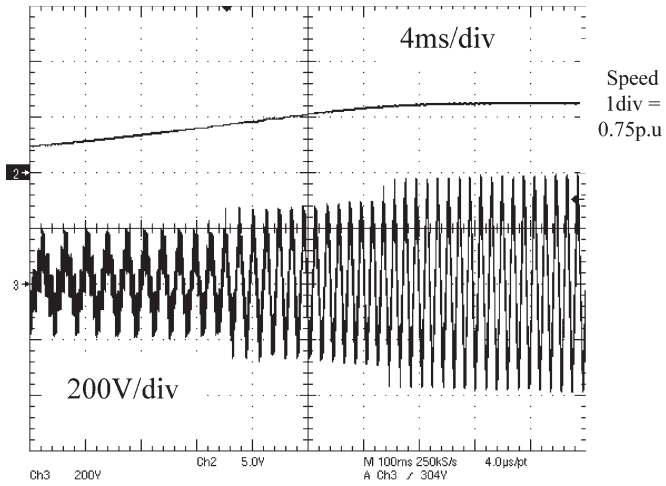



Fig. 15. Motor phase voltage during speed transient.

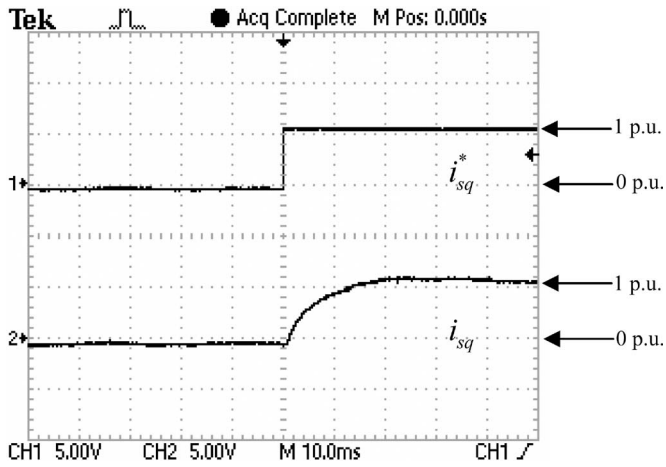



Fig. 16. Torque current $(i_{sq})$ for step change in torque-current command $(i^*_{sq})$.

during the transients. Fig. 16 shows the response of the torque current $(i_{sq})$ for the same transient of a step change in torque-current command $(i^*_{sq})$. This figure shows that the $i_{sq}$ has a response time constant of 4 ms as per the design.

## VI. Conclusion

A series connection of three-level inverters has been proposed for a medium-voltage sensorless vector control SQIM drive with increased voltage capacity. The topology ensured high-power operations with medium-voltage output having several voltage levels. The reduction in the ratings of the dc-bus capacitor and reduced imbalance problems in the dc bus [18]–[20] are some of the advantages of the proposed topology over the existing topologies. The disadvantage of the proposed topology is that it requires additional output transformers which introduce additional cost and losses. However, these transformers do not have complex underutilized windings like that required in cascaded H-bridge topologies [6]–[8].

A scaled-down (10 kVA) laboratory protomodel of this inverter is developed for vector-controlled SQIM drive application. The topology is tested for SQIM drive application in the frequency range near 8–50 Hz due to the problems of sensorless

control in low-frequency operations and also due to the problems of low-frequency operation of a standard transformer.

Different PWM strategies are used for this inverter control. Using the feedforward control strategy for the motor, a first-order response is achieved for the motor currents with a time constant of 4 ms. The motor terminal voltage shows a number of steps at different operating conditions. Therefore, the life of the motor is also expected to be very high due to the low applied $dv/dt$. The modularity of the proposed drive gives flexibility in different high-power applications. If one module of the topology fails, the inverter can operate at reduced power level similar to the single-phase H-bridge topology [6]. The topology is targeted for frequency of above 10 Hz. However, for low-frequency operation, its concerns can be addressed by having a current control on the primary side of the output transformers.

## APPENDIX
## MOTOR PARAMETERS

Rated power—7.5 hp.
Rated frequency—50 Hz.
Rated speed—1435 r/min.
Number of poles—4.
Stator line voltage—415 V.
Rated line current–10.8 A.

$$R_s = 1.3\,\Omega \quad R_r = 0.476\,\Omega$$
$$L_0 = 0.1310H \quad \sigma_s = 0.0396H \quad \sigma_r = 0.0396H.$$

## REFERENCES


[1] F. Wang, "Motor shaft voltages and bearing currents and their reduction in multilevel medium-voltage PWM voltage-source-inverter drive applications," *IEEE Trans. Ind. Appl.*, vol. 36, no. 5, pp. 1336–1341, Sep./Oct. 2000.

[2] S. Chen and T. A. Lipo, "Bearing currents and shaft voltages of an induction motor under hard- and soft-switching inverter excitation," *IEEE Trans. Ind. Appl.*, vol. 34, no. 5, pp. 1042–1048, Sep./Oct. 1998.

[3] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 36–44, Jan./Feb. 1999.

[4] A. Muetze and A. Binder, "Calculation of circulating bearing currents in machines of inverter-based drive systems," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 932–938, Apr. 2007.

[5] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, control and applications," *IEEE Trans. Power Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[6] P. W. Hammond, "A new approach to enhanced power quality for medium voltage drives," *IEEE Trans. Ind. Appl.*, vol. 33, no. 1, pp. 202–208, Jan./Feb. 1997.

[7] R. Teodorescu, F. Blaabjerg, J. K. Pederson, E. Cengelci, and P. N. Enjeti, "Multilevel inverter by cascading industrial VSI," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 832–838, Aug. 2002.

[8] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral point clamped inverter," *IEEE Trans. Ind. Appl.*, vol. 17, no. 5, pp. 518–523, Sep./Oct. 1981.

[9] J.-S. Lai and F. Z. Peng, "Multilevel converters—A new breed of power converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, May/Jun. 1996.

[10] G. Cararra, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A new multilevel PWM method: A theoretical analysis," *IEEE Trans. Power Electron.*, vol. 7, no. 3, pp. 497–505, Jul. 1992.

[11] A. M. Trzynadlowski, R. L. Kirlin, and S. Legowski, "Space vector PWM technique with minimum switching losses," *IEEE Trans. Ind. Electron.*, vol. 44, no. 2, pp. 173–181, Apr. 1997.

[12] Y. S. Lai and S. R. Bowes, "Optimal bus-clamped PWM techniques for three-phase motor drives," in *Proc. Annu. Conf. IEEE Ind. Electron. Soc.*, Busan, Korea, Nov. 2–6, 2004, pp. 1475–1480.

[13] B. P. McGrath, D. G. Holmes, and T. A. Lipo, "Optimized space vector switching sequences for multilevel inverters," *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1293–1301, Nov. 2003.

[14] B. P. McGrath, D. G. Holmes, and T. Meynard, "Reduced PWM harmonic distortion for multilevel inverters operating over a wide modulating range," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 941–949, Jul. 2006.

[15] K. D. Hurst, T. G. Habetler, G. Griva, and F. Profumo, "Zero-speed tacholess IM torque control: Simply a matter of stator voltage integration," *IEEE Trans. Ind. Appl.*, vol. 34, no. 4, pp. 790–795, Jul./Aug. 1998.

[16] T. Ohtani, N. Takada, and K. Tanaka, "Vector control of induction motor without shaft encoder," *IEEE Trans. Ind. Appl.*, vol. 28, no. 1, pp. 157–164, Jan./Feb. 1992.

[17] S. Mukherjee and G. Poddar, "Fast control of filter for sensorless vector control SQIM drive with sinusoidal motor voltage," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2435–2442, Oct. 2007.

[18] C. Newton and M. Summer, "Novel technique for maintaining balanced internal DC link voltages in diode-clamped five-level inverters," *Proc. Inst. Elect. Eng.—Elect. Power Appl.*, vol. 146, no. 3, pp. 341–349, May 1999.

[19] N. S. Choi, J. G. Cho, and G. H. Cho, "A general circuit topology of multilevel inverter," in *Proc. 22nd Annu. IEEE Conf. ESC*, Jun. 24–27, 1991, pp. 96–103.

[20] M. Marchesoni and P. Tenca, "Diode-clamped multilevel converters: A practicable way to balance DC-link voltages," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 752–765, Aug. 2002.

[21] W. Leonhard, *Control of Electrical Drives*. Berlin, Germany: Springer-Verlag, 1985.


**Suvajit Mukherjee** received the B.E. degree in electrical engineering from Bengal Engineering College, Shibpur, India, in 2001, the M.E. degree in electrical engineering from Jadavpur University, Kolkata, India, in 2004, and the Ph.D. degree in electrical engineering from the Indian Institute of Technology, Kharagpur, India, in 2008.

Since 2007, he has been with the Research and Development Center, Emerson Network Power India Private, Ltd., Thane, India. His fields of interests are multilevel converters, control of high-power drives, and sensorless control of ac motors.

**Gautam Poddar** received the B.E. degree in electrical engineering from Bengal Engineering College, Calcutta University, Kolkata, India, in 1992, the M.Tech. degree in electrical engineering from the Indian Institute of Technology, Kharagpur, India, in 1994, and the Ph.D. degree in electrical engineering from the Indian Institute of Science, Bangalore, India, in 2002.

From 1995 to 2004, he was with the Power Electronics Group of the Electronics Research and Development Center of India, where he was working in the field of power electronics and drives. In 2004, he joined the Department of Electrical Engineering, Indian Institute of Technology, Kharagpur, where he is currently an Assistant Professor. His fields of interest are control of high-power drives, sensorless control of ac motors, and active power filters.

Dr. Poddar was the recipient of the Indian National Academy of Engineers Young Engineers Award in 2003.