

Theoretical Analysis of Power Flow and Stored Energy in the Capacitor of Neutral-Point-Clamped Modular Multilevel Converter

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Abstract

This paper describes theoretical analysis of a power flow and a total stored energy in the capacitor of a neutral-point-clamped modular multilevel converter (NPC-MMC). The NPC-MMC consists of both a three-level structure with common DC capacitors and chopper cells. It requires only half of chopper cells compared to the conventional MMC.

In this paper, at first, theoretical analysis reveals the NPC-MMC can supply the AC power from not only the cells but also common DC capacitors. The direct power flow between the DC capacitors and the AC side brings 48% reduction of the total stored energy in the cell capacitors and the DC capacitors to the conventional MMC.

Secondary, the 10-kVA experimental circuit using low-voltage MOSFETs validates the capacitor energy analysis. Measured efficiency reaches extremely high value of 99.3%. Therefore, it requires neither heat sink nor cooling fans. These experimental results show that the NPC-MMC can realize both downsizing and very high efficiency conversion.

Introduction

A low-voltage grid-connected converter has been widely used for photovoltaic power conditioning systems (PV-PCS), uninterruptible power systems (UPS) and regenerative power converters. As a converter topology, a two-level converter has usually applied for its application because the number of its switching devices is small and it can be easily controlled. However, large and high-cost filters are required for keeping a grid code because of large harmonic components.

Multilevel converters, which generate a low harmonic output voltage, have attracted great interests[1]. A very small filter is enough for multilevel converters to suppress a harmonic distortion and electromagnetic interference. A withstand voltage of switching device in a multilevel converter is reduced to $1/(N-1)$ (N is the number of voltage levels). In [2], power losses can be also reduced by increasing the number of voltage levels in case that MOSFETs are employed even if the number of the switch is increased.

A modular multilevel converter (MMC), which consists of a series-connected unit converters with a capacitor such as chopper cells and bridge cells, have been proposed[3] and its operation and controls have been discussed in [4]. The number of levels of the MMC can easily increase by increasing the number of cells. But the very large cell capacitors are required to suppress a fundamental frequency voltage ripple of the cell capacitors[5].

To reduce the cell capacitors, several circuit configurations have been presented. An alternate arm converter (AAC)[6] consists of the switching device connected in series to a series-connected unit converters to reduce the number of the cells. But the cell for the AAC is a full-bridge cell. So the total number of the switching devices increases. A modular embedded multi-level converter (MEMC)[7]-[9] is based on a three-level structure with thyristors or IGBTs and the series-connected unit converters. A voltage of a series-connected unit converters of MEMC is roughly half of compared with the MMC.

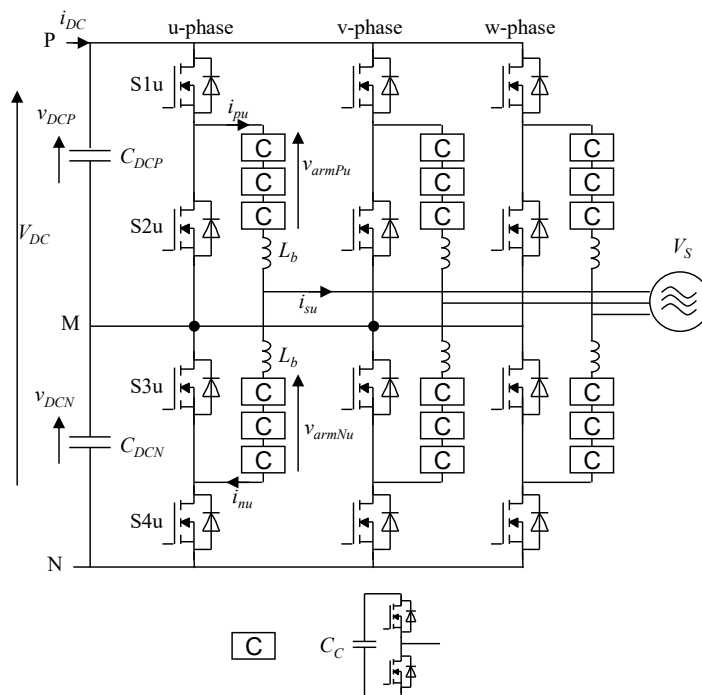


Fig. 1 Circuit configuration of an NPC-MMC.

Thus, MEMC only needs half the number of the cell. In the case of using thyristors, MEMC also needs some full-bridge cells to output some negative voltage to commutate the thyristors[9].

A neutral-point-clamped MMC (NPC-MMC) is referred to as a one of circuit topology which is based on a MEMC using a three-level structure with self-commutated devices such as IGBTs and two DC capacitors and its control method is discussed in [10]. The NPC-MMC also has the advantage of the half number of the cells, however, it is not clear how much the capacitor energy of the NPC-MMC including the cells and the DC capacitor is required.

This paper describes theoretical analysis of a power flow and a total stored energy in the capacitor of the NPC-MMC. It is explained the reason that a total stored energy is reduced by a power flow analysis. Theoretical analysis reveals the NPC-MMC can supply the AC power from not only the cell but also DC capacitor. That enables 50% reduction of a stored energy because the DC capacitor is common in three phase to cancel out the fundamental frequency voltage or energy ripple. Experimental circuit using low-voltage MOSFETs validates capacitor energy analysis and is confirmed that the NPC-MMC can bring both downsizing and high efficiency.

Neutral-point-clamped modular multilevel converter

Fig. 1 shows a configuration of the three phase NPC-MMC. The series-connected unit converters, which is referred to as the converter arm in this paper, is connected to the AC output terminals of two high-voltage chopper consisting of high voltage switches S1u-S4u. The DC voltage V_{DC} is divided by two common DC capacitors C_{DCP} and C_{DCN} . The neutral point M is common in three phase. The converter arms of a positive side and negative side are connected each other through buffer-reactors. Compared with the MMC, although additional DC capacitors and high-voltage switches are required, the number of the cell is reduced to 50% when the rated voltage of the cell is the same.

Fig. 2 describes a switching sequence of the high-voltage switches S1u-S4u and the voltage reference of the converter arms. The high-voltage switches, ignoring a voltage drop of the buffer-reactors, is synchronized with the grid line-to-ground voltage e_u . When the e_u is positive, S1u and S3u are turn on and S2u and S4u are turn off. At this period, the converter arm of the positive side generates a voltage of a difference between the DC capacitor voltage v_{DCP} and grid voltage e_u . On the other hand, the converter arm of the negative side outputs grid voltage e_u because it is connected to neutral point M. Therefore, the voltages of the converter arm are given as follows.

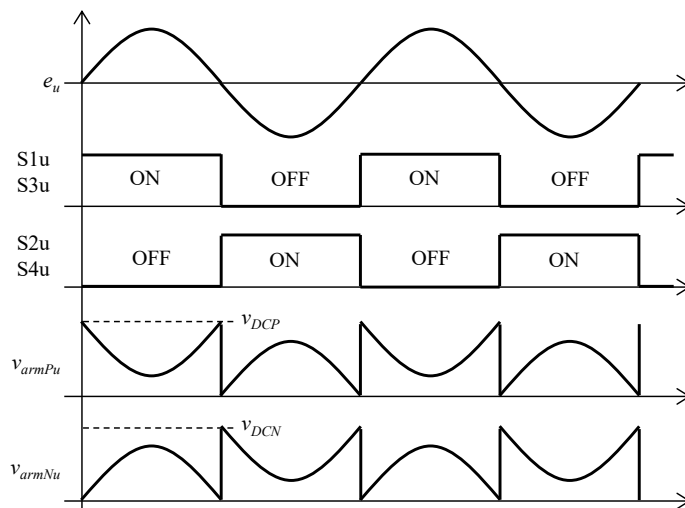


Fig. 2 Circuit configuration of an NPC-MMC.

$$v_{armPu} = \begin{cases} v_{DCP} - e_u & \cdots 0 \leq \omega t \leq \pi \\ -e_u & \cdots \pi \leq \omega t \leq 2\pi \end{cases} \quad (1)$$

$$v_{armNu} = \begin{cases} e_u & \cdots 0 \leq \omega t \leq \pi \\ e_u + v_{DCN} & \cdots \pi \leq \omega t \leq 2\pi \end{cases} \quad (2)$$

Since the DC capacitor voltage of v_{DCP} and v_{DCN} are controlled to half of the DC voltage V_{DC} , the maximum voltage of the converter arms is half of the DC voltage V_{DC} ; that is, the number of the cell in the NPC-MMC is half of that in the MMC.

Calculating Fourier series expansion from (1) and (2) gives

$$v_{armPu} = \frac{V_{DC}}{4} - \left(\sqrt{\frac{2}{3}} V_s - \frac{V_{DC}}{\pi} \right) \sin \omega t + \frac{V_{DC}}{\pi} \sum_{n=2} \frac{\sin[(2n-1)\omega t]}{2n-1}. \quad (3)$$

From second term of (3), we can see that the converter arm needs not to output all the grid voltage. It has only to output the difference between the grid voltage and the voltage of a fundamental frequency component generated by DC capacitors.

Power flow analysis of the NPC-MMC

The current through the converter arm includes, the same as the MMC, not only an AC current component but also a circulating current to keep the cell capacitor voltages. The circulating current in the NPC-MMC flows through the converter arm of the positive and negative side and the DC capacitor and is given by

$$i_p = \frac{\sqrt{2}}{2} I_s \sin(\omega t + \theta) + I_Z. \quad (5)$$

$$i_n = -\frac{\sqrt{2}}{2} I_s \sin(\omega t + \theta) + I_Z. \quad (6)$$

The first term of (5) and (6) represents an AC line current, which is provided in half from the positive converter arm and negative converter arm. The second term shows the DC circulating current. Given a periodic average power multiplying (3) and (5) equals to zero, I_Z is given by

$$I_Z = \frac{P}{V_{DC}} \left(\frac{2}{3} - \sqrt{\frac{2}{3}} \frac{V_{DC}}{\pi V_s} \right). \quad (7)$$

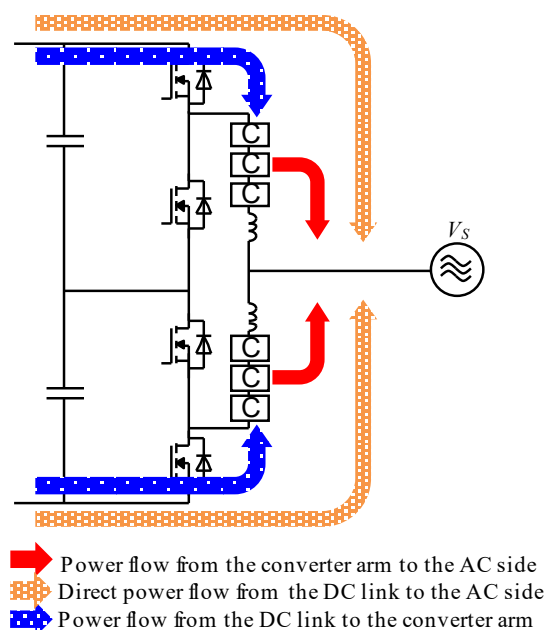


Fig. 3: A power flow in an NPC-MMC.

The DC circulating current in the NPC-MMC is smaller than that in the conventional MMC, which is given by

$$I_{Z-MMC} = \frac{P}{3V_{DC}}, \quad (8)$$

owing to direct power flow from the DC capacitor to the AC side. For example, provided the condition of $\sqrt{\frac{2}{3}}V_s = \frac{V_{DC}}{2}$, I_Z in the NPC-MMC is expressed as (8) and 27% smaller than that in the MMC.

$$I_Z = \frac{P}{3V_{DC}} \left(2 - \frac{4}{\pi} \right) = 0.73 \times \frac{P}{3V_{DC}}. \quad (9)$$

A power flow in the NPC-MMC is shown in Fig. 3. The power flow consists of three components. First is a power flow from the converter arm (or the cells) to the AC side, which the conventional MMC also has. Second is a direct power flow from the DC capacitor (or the DC link) to the AC side. Third is a power flow from the DC capacitor to the converter arm. That means the circulating current conveys an average power from the DC capacitor to the cells, a power corresponding to that from the converter arm to the AC side.

A role of the two DC capacitors C_{DCP} and C_{DCN} is as follows.

- An energy buffer for an average power exchanged directly with the AC side.
- An energy absorber of simultaneous power ripple exchanged directly with the ac side.

Note that the conventional MMC has no dc capacitor connected to the DC link because all the power to the AC side is supplied from the converter arm.

Total stored energy in the capacitors of the NPC-MMC

Stored energy in the cell capacitors

When a voltage and a current of the converter arm are controlled as (3) and (5) respectively, the energy in the converter arm (or the cells) is given by

$$W_P = \int v_{armP} \cdot i_P dt. \quad (10)$$

Here, the chopper cell voltage v_{CP} is represented as following equation using first order approximation of Taylor series.

Table 1 Parameters of the calculation.

Rated power	P	10 kVA
Line-to-line voltage	V_S	200 V
Rated system current	I_S	28.9 A
System frequency	f	50 Hz
DC link voltage	V_{DC}	350 V
Cell capacitor at $k=0.1, P=10$ kW	C_C (NPC-MMC)	8.26 mF
Cell capacitor at $k=0.1, P=10$ kW	C_C (MMC)	6.21 mF
Cell capacitor voltage	V_{C0}	65 V
High-voltage capacitor at $k=0.1, P=10$ kW	C_{DCP}, C_{DCN}	0.58 mF
Number of cells	N	3

$$v_{CP} = \sqrt{\frac{2}{NC_C} W_P} \approx V_{C0} + \frac{\widetilde{W}_P}{NC_C V_{C0}}, \quad (11)$$

where N is the number of the cells in one converter arm, V_{C0} is the time average voltage of v_{CP} , and \widetilde{W}_P represents an energy ripple (or ac component) of W_P . The ripple voltage of the chopper cell is proportional to energy ripple.

Using (11), the cell capacitance that suppresses the ripple voltage less than kV_{C0} is given by

$$C_C = \frac{\Delta W_P}{kNV_{C0}^2}, \quad (12)$$

where k is allowable variation limit and ΔW_P represents an energy ripple width of W_P . The analysis of the negative arm is the same as that of the positive arm. As a result, the stored energy in the cell capacitors is as follows:

$$W_{cell} = 6N \cdot \frac{1}{2} C_C V_{C0}^2 = \frac{3\Delta W_P}{k}. \quad (13)$$

Stored energy in the DC capacitors

For the common DC capacitor, the current flowing into it is given by

$$i_{DCP} = I_{DC} - (S1u \cdot i_{pu} + S1v \cdot i_{pv} + S1w \cdot i_{pw}), \quad (14)$$

where $S1$ is a switching function shown that on-state is one and off-state is zero. (14) means the current in the DC capacitor is the rectified arm current by high-voltage switches. Since the phase difference between $S1u$, $S1v$ and $S1w$ is 120 degrees, the fundamental frequency component of the arm current is cancel out.

Supposed the DC capacitor voltage is constant as the average value $V_{DCP0} = V_{DC}/2$, the energy in the DC capacitor is represented as

$$W_{DCP} = \int V_{DCP0} \cdot i_{DCP} dt. \quad (15)$$

Similar to the cell capacitor, the DC capacitance that suppresses the ripple voltage less than kV_{DCP0} is given by

$$C_{DCP} = \frac{\Delta W_{DCP}}{kV_{DCP0}^2}, \quad (16)$$

where V_{DCP0} is the time average voltage of v_{DCP} and ΔW_{DCP} represents an energy ripple width of W_{DCP} . The stored energy in the DC capacitors is as follows:

$$W_{DC} = 2 \cdot \frac{1}{2} C_{DCP} V_{DCP0}^2 = \frac{\Delta W_{DCP}}{k}. \quad (17)$$

Calculated stored energy in the NPC-MMC

Using the equation of (13) and (17), the total stored energy in the NPC-MMC is given by

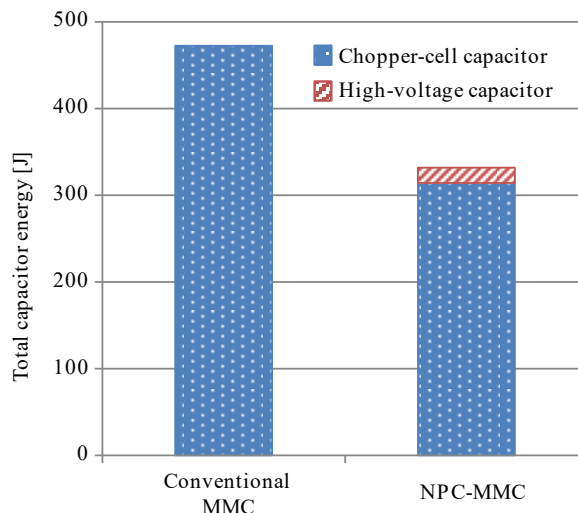


Fig. 4: Comparison of the total energy stored in the capacitors (P=10 kW).

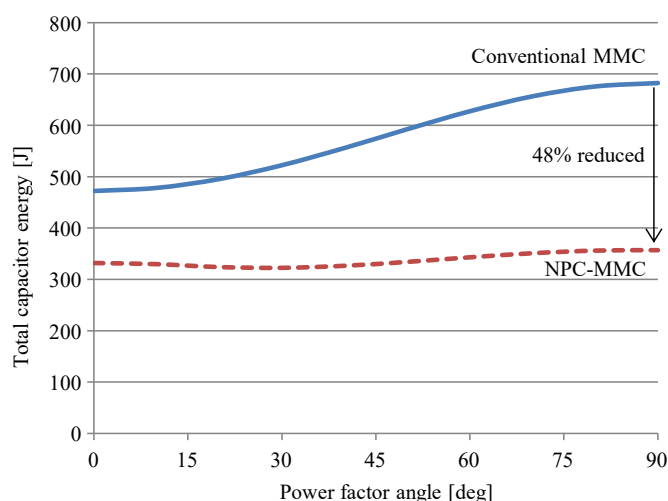


Fig. 5: Total energy stored in the capacitors of the chopper-cell and DC capacitors.

$$W_{NPC-MMC} = W_{cell} + W_{DC} = \frac{3\Delta W_P + \Delta W_{DCP}}{k}. \quad (18)$$

The total stored energy is proportional to the energy ripple width and inversely proportional to the allowable variation limit.

Fig. 4 and Fig. 5 show the calculated total stored energy in the NPC-MMC and the conventional MMC when the power rating is 10 kVA and the allowable variation limit is set to plus-minus 5% ($k=0.1$). Other parameters of the calculation are shown in Table 1. The conventional MMC is calculated as following equations (19)(20)(21):

$$V_{MMC} = \frac{V_{DC}}{2} - e_u, \quad (19)$$

$$i_{p-MMC} = \frac{\sqrt{2}}{2} I_s \sin(\omega t + \theta) + \frac{P}{3V_{DC}}, \quad (20)$$

$$W_{MMC} = \frac{3\Delta W_{P-MMC}}{k}. \quad (21)$$

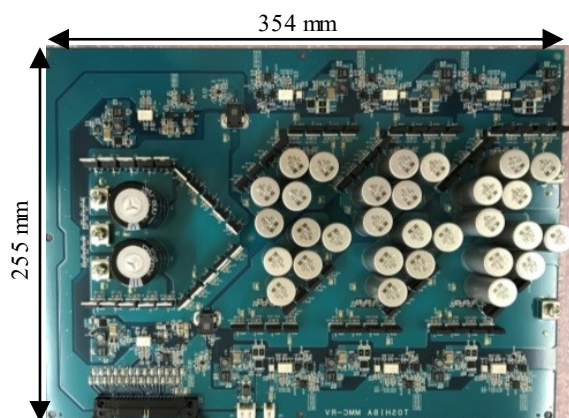


Fig. 6: Photo of the converter circuit board (1 phase).

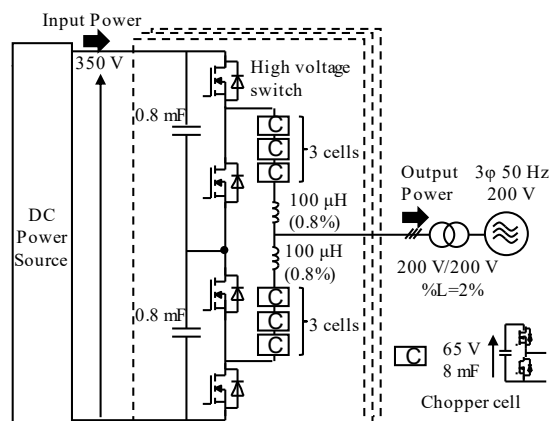


Fig. 7 The experimental circuit configuration.

Table 2 Parameters of the experimental setup.

Rated power	P	10 kVA
Line-to-line voltage	V_S	200 V
Rated AC line current	I_S	28.9 A
System frequency	f	50 Hz
DC link voltage	V_{DC}	350 V
Cell capacitor	C_C	8 mF
Cell capacitor voltage	V_{CO}	65 V
DC capacitor in one phase	C_{DCB}, C_{DCN}	0.8 mF
DC capacitor voltage	V_{DCP}, V_{DCN}	175 V
Buffer-reactor	L_b	0.1 mH (0.4%)
Switching frequency of the cell	f_{sw}	6.6 kHz
Number of cells	N	3

When the power factor angle is zero ($P = 10$ kW), the total stored energy of the NPC-MMC is reduced to 70% of the MMC as shown in Fig. 4. This is because the NPC-MMC has a direct power flow from DC link to AC side not passing through the cells where it causes a single-phase instantaneous power ripple. In the case of three phase converter, the fundamental frequency components of the direct power from DC link to AC sides are cancelled out on the DC capacitors. Although the sixth frequency component remains, the DC capacitors are much smaller than the chopper cell capacitors.

Fig. 5 shows that the total stored energy of the NPC-MMC does not increase during a reactive power operation. For the MMC, however, the more reactive power is generated, the larger capacitor is need to suppress the voltage ripple. In general, the circuit is designed considering a maximum energy of every operation. Therefore, the total stored energy of the NPC-MMC is reduced by 48% to the MMC if the power factor angle is 90 degrees ($Q = 10$ kvar).

Experimental results

Experimental circuit

This paper verify the analysis of the capacitor stored energy with an experimental circuit of 10 kVA using low-voltage MOSFETs. The experimental circuit configuration and manufactured converter circuit board of the NPC-MMC is shown in Fig. 6 and Fig. 7, respectively. It is connected to a DC power supply and 200 V AC grid through a delta-connected transformer, which is for the convenience of the test site and has a leakage inductance of 2%. The parameters of the experimental setup are shown in Table 2.

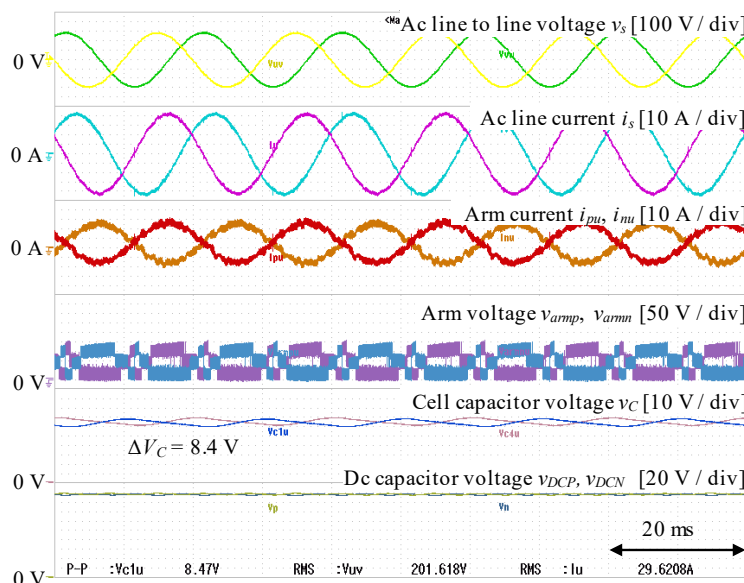


Fig. 8: Experimental waveforms of the NPC-MMC at the active power operation (10 kW).

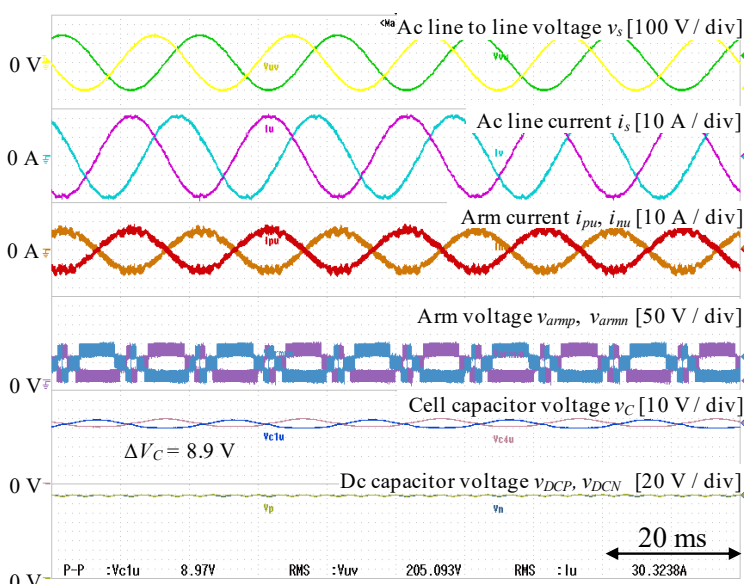


Fig. 9: Experimental waveforms of the NPC-MMC at the reactive power operation (10 kvar).

The MOSFETs have neither heat sink nor cooling fans because the on-state resistance of the MOSFET and its switching frequency are very low. The frequency of the buffer-reactor current is $Nf_{sw} = 20$ kHz. This paper set the equivalent switching frequency to be above the audible range frequency.

Rated operation

Fig. 8 shows experimental waveforms of the NPC-MMC at the 10-kW active-power operation. The AC line currents are controlled to sinusoidal waves with low harmonic components. The voltages of the cell capacitors and the DC capacitors are also controlled to be constant of a reference value. These contain the fundamental frequency ripples and the sixth frequency ripples, respectively. The peak-to-peak ripple voltage of the cell capacitors is 8.4 V ($k=0.130$) and the total stored energy of the experimental circuit is 378 J (Cell capacitors: 304.2 J, DC capacitors: 73.5 J). These results agree well with the analytical results.

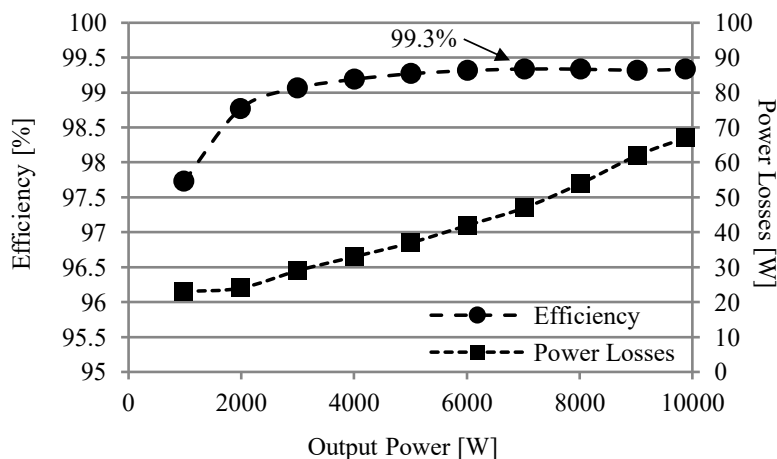


Fig. 10: Measured conversion efficiency and power losses.

Fig. 9 shows experimental waveforms at the reactive power operation. In this condition, the peak-to-peak ripple voltage of the cell capacitors is 8.9 V ($k=0.137$). The ripple voltage at the reactive power operation is almost the same as that at the active power operation as shown in Fig. 5.

In the case of the active power operation, the arm current has a DC component which is the circulating current to make a power flow from the DC capacitor to the cell capacitors. For the NPC-MMC, since the cell capacitors need only a part of a total energy to the AC side, the circulating current becomes 6 A according to (7) and Table 2. In contrast, according to (8), the cell capacitors of the MMC required the circulating current of 9.5 A to keep the cell capacitor voltage constant. It means the conduction loss of the converter can also decrease.

Power losses

The measured power losses and efficiency are shown in Fig. 10. The power losses contain not only at MOSFETs and capacitors but also at buffer-reactors and gate losses of the MOSFETs. Keep in mind that the power losses at the transformer is not included. On a wide power range, the efficiency reaches over 99% and the maximum efficiency is 99.3%. As a result, without any heat sink or cooling fans, the surface temperature of each MOSFET can be almost the same as room temperature. Distributed arrangement of the MOSFET on the circuit board is also a key to realize heat-sink less structure.

As the output voltage of the NPC-MMC is multilevel, the inductance of the buffer-reactor can be reduced with a low switching frequency. Lower inductance value also leads to reducing copper losses because the turn number is proportional to the square of an inductance value. Moreover, applying the low-voltage MOSFETs, the on-state losses that is proportional to the square of the output power becomes very low despite no increasing cost. Therefore, the NPC-MMC realizes very high efficient conversion.

Conclusion

This paper describes theoretical analysis of a power flow and a total stored energy in the capacitor of the NPC-MMC. The direct power flow between the DC capacitors and the AC side brings 48% reduction of the total stored energy in the cell capacitors and the DC capacitors to the conventional MMC. Experimental results using the manufactured circuit boards of 10 kVA agree well with the analytical results and show that the NPC-MMC can realize very high efficiency conversion.

References

- [1] Fang Zheng Peng, "A generalized multilevel inverter topology with self voltage balancing," in *IEEE Transactions on Industry Applications*, vol. 37, no. 2, pp. 611-618, Mar/Apr 2001.
- [2] Y. Kashihara and J. Itoh, "Power losses of multilevel converters in terms of the number of the output voltage levels," 2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA), Hiroshima, 2014, pp. 1943-1949.
- [3] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," *2003 IEEE Bologna Power Tech Conference Proceedings*, 2003, pp. 6 pp. Vol.3-.
- [4] M. Hagiwara and H. Akagi, "Control and Experiment of Pulsewidth-Modulated Modular Multilevel Converters," in *IEEE Transactions on Power Electronics*, vol. 24, no. 7, pp. 1737-1746, July 2009.
- [5] K. Ilves, S. Norrga, L. Harnefors and H. P. Nee, "On Energy Storage Requirements in Modular Multilevel Converters," in *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 77-88, Jan. 2014.
- [6] M. M. C. Merlin et al., "The Alternate Arm Converter: A New Hybrid Multilevel Converter With DC-Fault Blocking Capability," in *IEEE Transactions on Power Delivery*, vol. 29, no. 1, pp. 310-317, Feb. 2014.
- [7] Di Zhang, Multilevel Converter System, U. S. Patent 2014/0092660, 2014-4-3.
- [8] Di Zhang, Multilevel Converter System, U. S. Patent 2014/0092661, 2014-4-3.
- [9] D. Zhang, R. Datta, A. Rockhill, Q. Lei and L. Garces, "The modular embedded multilevel converter: A voltage source converter with IGBTs and thyristors," 2016 IEEE ECCE, Milwaukee, WI, 2016, pp. 1-8.
- [10] R. Hasegawa, S. Tashiro and D. Suzuki, "A Proposal of Control Method for Regulating Capacitor Voltages of Neutral Point Clamped Modular Multilevel Converter," PCIM Asia 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Shanghai, China, 2017, pp. 1-6.