A Comparative Performance Study of Advanced PLLs for Grid Synchronization

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***Abstract*—The interfacing of renewable energy sources (RESs) into power system through power electronic converters is being increased in microgrid. The control and integration of RESs require an accurate fundamental frequency positive sequence (FFPS) component extraction methods to enhance the disturbance rejection capability of SRF-PLL for various grid conditions. The extraction of FFPS components based on second order generalized integrator (SOGI), cascaded delayed signal cancellation (CDSC) and multiple delayed signal cancellation (MDSC) PLLs are reviewed and their extraction accuracy is evaluated for various grid conditions based on the quality of frequency in SRF-PLL. The performance comparison of these PLLs is presented based on the MATLAB simulation results.**

***Index Terms*—Cascaded delayed signal cancellation (CDSC), delayed signal cancellation (DSC), grid synchronization, multiple delayed signal cancellation (MDSC), phase locked loop (PLL), second order generalized integrator (SOGI).**

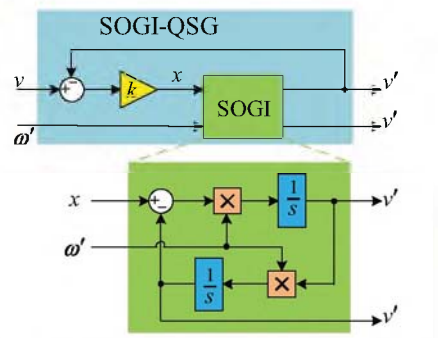

Fig. 1: General structure for SOGI based QSG

I. Introduction

The integration of renewable energy sources (RESs) to the utility grid at the distribution side is being increased due to fossil fuels depletion and the growing level of awareness on environmental concerns. The distributed energy sources (DERs) or RESs are interfaced to the grid with the help of power electronic converters comprising non-linear devices. The grid integration of RESs requires proper synchronization (i.e., accurate phase, magnitude and frequency of the grid voltage) with fast transient response for the reliable and quality power transfer of RESs to the grid. The conventional method for the grid synchronization is the synchronous reference frame phase locked loop (SRF-PLL), which extracts the phase angle and frequency of the grid voltage. The dynamic performance of SRF-PLL is well satisfactory only under the balanced and distortion free grid voltages [1]. However, the rise in RESs integration and the usage of non-linear loads at the distribution side can lead to phase angle jump, harmonics and distortions in grid voltage. Under these conditions, the dynamic performance of SRF-PLL with high bandwidth deteriorates. The performance of SRF-PLL can be improved by the selection of low bandwidth but with a compromise in slow response speed.

In order to extract accurate phase angle information under these polluted grid conditions with a zero steady state error and quick response, the fundamental frequency positive sequence (FFPS) components are to be passed through SRF-PLL. There are different methods to extract FFPS components in the literature and they can be broadly classified into two. The first method is based on notch filters with instantaneous symmetrical components (ISC) theory. The fundamental and its quadrature signals are extracted using notch filters and then using ISC theory, the positive sequence components are derived. The second method is based on the delay operators which inherently have a filtering capability. The quadrature signals can also be generated using delay operators on each phase but it may lead to inaccuracy due to large requirement of delay operators especially while working on a digital platform. The examples for the former method are enhanced PLL (EPLL), second order generalized integrator (SOGI) and for the later method are cascaded delayed signal cancellation (CDSC), multiple delayed signal cancellation (MDSC) methods.

Three EPLLs are used, one for each phase, to obtain FFPS components and a fourth EPLL is used to extract phase angle of grid voltage [2]. The performance of EPLL is insensitive to the frequency variations because it is a frequency adaptive notch filter. In order to reduce the number of EPLLs, a dual EPLL (DEPLL) is proposed in $\alpha\beta$ frame with an assumption that $\alpha\beta$ components of grid voltages are in quadrature to each other [3]. However, it is no longer true for unbalanced grid system. This drawback can be overcome by using SOGI as quadrature signal generator (QSG) [4]. In recent years, SOGI, CDSC and MSDC based PLLs are gaining popular because of their own merits. However, each PLL has its own demerits and hence this paper presents a brief review on these PLLs with basic principle concepts of each. This may help the academic researchers to further enhance the performance of PLLs for power system applications. In addition to this, the performance of these advanced PLLs for various grid conditions are studied and compared using MATLAB simulations. This would be helpful for engineers to choose a suitable PLL based on the application and the available resources.

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II. Review on Advanced PLLs

Over the past decade, power quality is being deteriorated severely with the proliferation of RESs and non-linear loads into power system. In order to tackle this issue, there have been many attempts in the recent years, to enhance the disturbance rejection capability of SRF-PLLs. Few such PLLs with enhanced disturbance rejection capability are SOGI, CDSC and MDSC based PLLs. This section presents a brief overview of these PLLs.

A. Second Order Generalized Integrator Based PLL

A general structure for SOGI based QSG is shown in Fig. 1. The transfer functions of input signal v to its in-phase filtered signal v' and input signal v to its filtered quadrature signal v'_q are respectively given in (1) and (2).

$$\begin{cases} \dfrac{v'(s)}{v(s)} = \dfrac{k\omega' s}{s^2 + k\omega' s + \omega'^2} \\ \left|\dfrac{v'}{v}\right| = \dfrac{k\omega'\omega}{\sqrt{(\omega'^2 - \omega^2)^2 + (k\omega'\omega)^2}} \\ \angle\dfrac{v'}{v} = \dfrac{\pi}{2} - tan^{-1}\left(\dfrac{k\omega'\omega}{(\omega'^2 - \omega^2)^2}\right) \end{cases} \quad (1)$$

$$\begin{cases} \dfrac{v'_q(s)}{v(s)} = \dfrac{k\omega'^2}{s^2 + k\omega' s + \omega'^2} \\ \left|\dfrac{v'_q}{v}\right| = \dfrac{k\omega'^2}{\sqrt{(\omega'^2 - \omega^2)^2 + (k\omega'\omega)^2}} \\ \angle\dfrac{v'_q}{v} = -tan^{-1}\left(\dfrac{k\omega'\omega}{(\omega'^2 - \omega^2)^2}\right) \end{cases} \quad (2)$$

Where, ω' is the resonant/natural frequency, ω is the frequency of a signal, and k is the gain which decides the transient response of a system. In general, v is the grid voltage in many applications of power system such as power quality improvement, grid integration of RESs, islanding detection and motor control. It is evident from (1) and (2) that SOGI-QSG offers band pass and low pass filtering features for v' and v'_q respectively. Furthermore, few more conclusions are made from (1) and (2) as following:

- Discrepancy between resonant frequency and the fundamental frequency of input signal doesnt fulfil the requirement of SOGI-QSG i.e., extraction of accurate fundamental frequency signal and its quadrature signal. To make SOGI-QSG frequency adaptive, SRF-PLL is used as shown in Fig. 2, which estimates the fundamental frequency of the input signal and it is fed to SOGI as a resonant frequency [5].
- Due to band pass filtering feature of SOGI-QSG for v', it passes the resonant frequency signals and attenuates but not nullifies other frequency signals. This results in impure sinusoidal shape in v for the polluted grid with dominant lower order harmonics and there is an error in phase angle and frequency estimation when v' is fed to SRF-PLL. However, dc component of the input is completely removed in v' by SOGI-QSG.

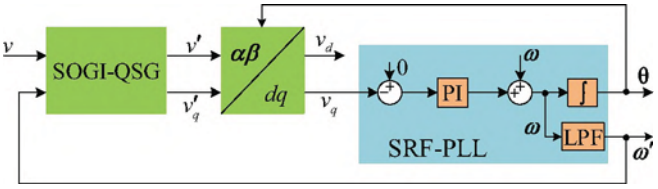

Fig. 2: General structure for frequency adaptive 1-ph SOGI-PLL

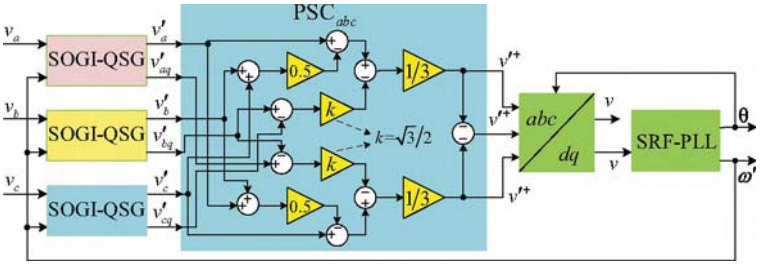

Fig. 3: General structure for frequency adaptive 3-ph SOGI-PLL

- Due to low pass filtering feature of SOGI-QSG for v'_q, it passes signals with frequency upto resonant frequency and attenuates signals with frequency beyond resonant frequency. This results in impure sinusoidal shape in v'_q for the polluted grid voltage with dominant lower order harmonics. In addition, the dc signal present in the sensed grid voltages due to control action distorts the v'_q and therefore error in phase angle and frequency estimation when such distorted v'_q is fed to SRF-PLL.
- v'_q always lags v' by 90° irrespective of resonant frequency and gain k [3].

For three phase system, three SOGI-QSGs, one per each phase, are used to extract fundamental and its orthogonal signal of each phase. From these extracted signals, FFPS components

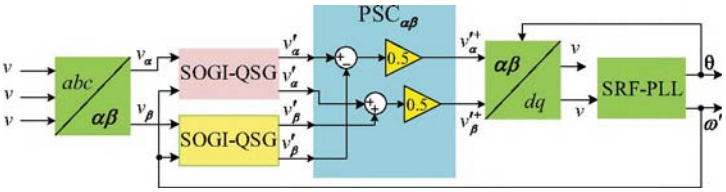

Fig. 4: General structure for frequency adaptive DSOGI-PLL

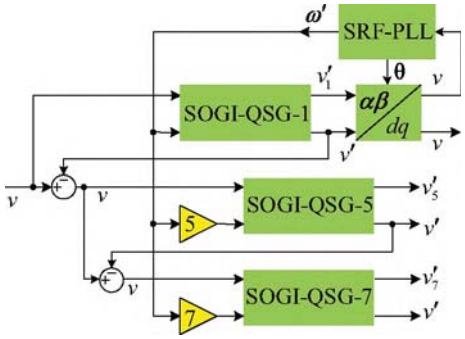

Fig. 5: General structure for frequency adaptive 1-ph MSOGI-PLL

are found based on ISC theory as given in (3) and they are fed to SRF-PLL as shown in Fig. 3.

$$\begin{cases} v_a'^{+} = \frac{1}{3}\left[\left\{v_a' - \frac{1}{2}(v_b' + v_c')\right\} - \frac{\sqrt{3}}{2}\left\{v_{bq}' - v_{cq}'\right\}\right] \\ v_b'^{+} = -v_a'^{+} - v_c'^{+} \\ v_c'^{+} = \frac{1}{3}\left[\left\{v_c' - \frac{1}{2}(v_a' + v_b')\right\} - \frac{\sqrt{3}}{2}\left\{v_{aq}' - v_{bq}'\right\}\right] \end{cases} \quad (3)$$

Analyzing system signals in $\alpha\beta$ reference frame reduces the number of SOGI-QSGs to two and it is named as a dual SOGI (DSOGI) based PLL which is shown in Fig. 4. This idea is same as in DEPLL but in DEPLL, the β component of input signal is considered as a quadrature to the α component of input signal. However, this is not valid for unbalanced systems. This problem is resolved in DSOGI based PLL by inferring only frequency information from the PLL. The positive sequence components in $\alpha\beta$ reference frame is also obtained using ISC theory as given below [5],

$$\begin{cases} v_\alpha'^{+} = \frac{1}{2}\left(v_\alpha' - v_{\beta q}'\right) \\ v_\beta'^{+} = \frac{1}{2}\left(v_{\alpha q}' + v_\beta'\right). \end{cases} \quad (4)$$

In power system, extraction of particular harmonic frequency signal is necessary for fault analysis as well as for the effective control of custom power devices. This can be achieved using multiple SOGI (MSOGI) based PLL which is shown in Fig. 5. The SOGI-QSG-h is the one which is used for h^{th} harmonic frequency signal extraction and it must not be fed with the signals with lower than h^{th} harmonic frequency due to low pass filter characteristic of SOGI-QSG for v_q'. In Fig. 5, it is shown that the input of SOGI-QSG-7 is obtained by subtracting outputs of its preceding SOGI-QSGs (i.e., for $h = 1$ and 5) from the actual input. For any reason, if the actual signal contains any of the $2^{nd}, 3^{rd}, 4^{th}$ and 6^{th} harmonic frequencies, then the extracted 7^{th} harmonic frequency signal is not accurate. Even if SOGI-QSGs are used for extraction of all harmonic frequency signals (i.e., from $h = 1$ to 6), there will be a considerable discrepancy between extracted 7^{th} harmonic frequency component by SOGI-QSG-7 and the 7^{th} harmonic frequency component of actual input signal. Since, output of SOGI-QSG-h contains dominantly h^{th} frequency signals and partially other frequency signals. For instance in Fig. 5, output of SOGI-QSG-1 has fundamental as well as fraction of 5^{th} and 7^{th} harmonic frequency components which results in inaccurate input for the later SOGI-QSGs (i.e., for $h = 5$ and 7). To overcome this issue for some extent, the input signal of each SOGI-QSG is calculated by subtracting the output of all other SOGI-QSGs from the original input signal [6], [7].

B. Cascaded Delayed Signal Cancellation Based PLL

In order to eliminate a particular frequency signal $v_h(t)$, perform the addition of actual signal and its out of phase signal i.e.,

$$DSC_n = \frac{1}{2}\left[v_h(t) + v_h(t - T/n)\right]$$

where T is the fundamental time period, $n \in N$ and this is called as delayed signal cancellation (DSC_n) operator [8]. The out of phase signal can be obtained with different delay times $\left(\frac{T}{n}\right)$. The minimum time delay required for the DSC_n operator is the period from time $t = 0$ to the time at which negative zero crossing of signal occurs. For instance, to eliminate a 4^{th} order harmonic frequency signal shown in Fig. 6, the possible delay times are $\frac{T}{8}, \left(\frac{T}{8} + \frac{T}{4}\right), \left(\frac{T}{8} + \frac{2T}{4}\right)$ and $\left(\frac{T}{8} + \frac{3T}{4}\right)$. To make it general, the possible delay times $\frac{T}{n}$ to eliminate the h^{th} harmonic frequency signal are

$$\frac{T}{n} = \frac{T}{2h} + k\frac{T}{h} \qquad \forall \;\; k < h - 0.5 \;\; \& \;\; k \in N_0. \quad (5)$$

In other words, for a known delay time, the eliminated harmonic signals are obtained from (5) and is given as,

$$h = nk + \frac{n}{2} \qquad \forall \;\; k, h \in N_0.$$

The harmonics eliminated by the DSC operators $DSC_2, DSC_4, DSC_8, DSC_{16}$ and DSC_{32} are $2k + 1$, $4k + 2, 8k + 4, 16k + 8$ and $32k + 16$ respectively. These operators are most often used because no single harmonic signal is eliminated by any two operators. The harmonics passed without attenuation by these DSC operators are $2k, 4k, 8k, 16k$ and $32k$ respectively. In order to eliminate all lower order harmonics, these DSCs are cascaded such that no signal is attenuated by any DSC operator. This forms a new operator named cascaded delayed signal cancellation ($CDSC_{2,4,8,16,32}$) operator [9]–[14]. This operator is intended to use in *dq* reference frame. If it is used in *abc* frame, then fundamental frequency component is eliminated which is to be fed to SRF-PLL for grid synchronization.

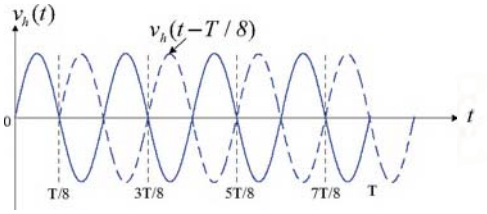

Fig. 6: Fourth order frequency signal and its delayed signal

The *dq* reference frames in vector space can be rotated at any frequency and in any direction. In general, these are rotated at fundamental frequency and in synchronism with the resultant vectors rotation. This leads to a balanced fundamental frequency components in *abc* frame appears as dc quantity in *dq* frame. The relationship between all the harmonic orders in *abc* and *dq* frames are given in Table I. From this table, it is observed that all odd order frequency signals in *abc* frame appears as even order harmonics in *dq* frame and vice versa. The $CDSC_{2,4,8,16,32}$ operator passes all $32k$ harmonic order frequency signals in *dq* frame whose equivalent harmonic order signals in *abc* frame are $32k \pm 1$. Therefore, $CDSC_{2,4,8,16,32}$ in *dq* frame effectively extracts the equivalent fundamental frequency component of *abc* frame. The total delay time of this CDSC operator is $31T/32$. To reduce the total delay time to $15T/16$, a $CDSC_{2,4,8,16}$ is used. However, it fails to eliminate all $16k$ harmonic frequency signals in *dq*

TABLE I: Harmonic order and nature in abc frame and dq frame, rotating at a speed of ω

Harmonic order (h) in abc frame $\forall\ k \in N_0$			**Harmonic order (h) in dq frame $\forall\ k \in N_0$**	
h	**sequence**	**nature**	**h**	**nature**
$6k+1$	positive	odd, balanced	$6k$	even
		odd, unbalanced	$6k$ & $6k+2$	
$6k-1$	negative	odd, balanced	$6k$	even
		odd, unbalanced	$6k$ & $6k-2$	
$3(2k+1)+1$	positive	even, balanced	$3(2k+1)$	odd
		even, unbalanced	$3(2k+1)$ & $3(2k+1)+2$	
$3(2k-1)-1$	negative	even, balanced	$3(2k+1)$	odd
		even, unbalanced	$3(2k+1)$ & $3(2k+1)-2$	
$3k\ \ \forall\ k \in N$	zero	odd/even, balanced	No dq components present	
		odd/even, unbalanced	$3k+1$ & $3k-1$	even/odd
0	—	dc, balanced	No dq components present	
		dc, unbalanced	$+1$	odd

frame whose equivalent harmonic order signals in abc frame are $16k \pm 1$. Thus, $CDSC_{2,4,8,16}$ requires lower bandwidth SRF-PLL when it is fed to SRF-PLL for grid synchronization. Moreover, CDSC operator in dq frame introduces time delay into the control loop of SRF-PLL. This in-loop delay will adversely affect the PLL dynamic performance. Therefore, in order to ensure high stability of SRF-PLL, the equivalent of CDSC operator in dq frame should be relocated into $\alpha\beta$ frame using the following expression [10].

$$\begin{bmatrix} DSC_n[v_{\alpha h}] \\ DSC_n[v_{\beta h}] \end{bmatrix} = \begin{bmatrix} cos\ h^*\theta & -sin\ h^*\theta \\ sin\ h^*\theta & cos\ h^*\theta \end{bmatrix} * \begin{bmatrix} DSC_n[v_{dh}] \\ DSC_n[v_{qh}] \end{bmatrix} \quad (6)$$

where, $DSC_n[v_{dqh}] = \frac{1}{2}\left[v_{dq}h(\omega t) + v_{dq}h(\omega t - T/n)\right]$, ω is the fundamental angular frequency, h is the harmonic order, $h^* = \pm\ h$ is the required positive sequence harmonic frequency component to be extracted by the CDSC operator, sign '+' is for positive sequence signals and sign '−' is for negative sequence signals and $\theta = \omega t$. The simplified expression of (6) is given in (7).

The execution of the CDSC operator is generally very efficient, because it requires only simple transport delay, multiplication, and summation operations in the digital controller. However, it will suffer from small discretization error when non-integer samples obtained for delay operation in any DSC operator [9], [12]. To get integer samples for delay operation, the total number of samples in a fundamental time period T must be chosen as an integer multiple of 32. The fundamental time period is not constant for many applications, one such application is electric aircraft power system which requires a power supply with a frequency range of 360 Hz to 900 Hz. Therefore, it is necessary to update T continuously for exact delay operation and it is done by using SRF-PLL as shown in Fig. 7. But, the updation in T may leads to non-interger samples in delay operation and thus small discretization error. To improve CDSC performance from this discretization error, linear interpolation method is proposed in [9].

In order to make CDSC as a QSG which is indeed necessary for single phase system, the idea of anticonjugate decomposition (ACD) proposed in [15] is used. Based on this concept, the α and β input components of CDSC are considered as 0 and the actual single phase signal respectively. The required frequency signal and its quadrature signals are obtained respectively at the β and α output terminals of CDSC with an attenuation of 50%. Thus, ACD based CDSC can also be used for single phase systems and its general diagram is shown in Fig. 8.

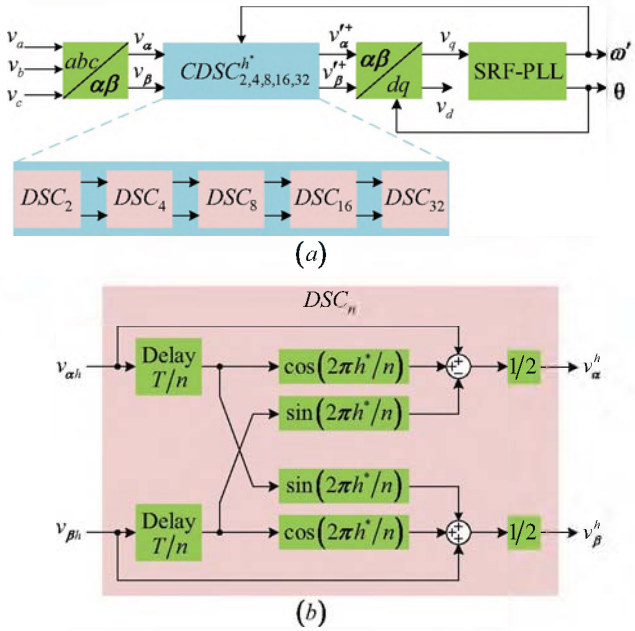

Fig. 7: (a). General structure for frequency adaptive 3-ph CDSC-PLL. (b) Time domain implementation of DSC_n operator.

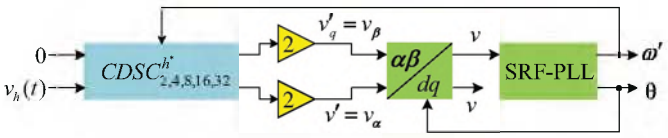

Fig. 8: General structure for frequency adaptive 1-ph ACD-CDSC-PLL.

C. Multiple Delayed Signal Cancellation Based PLL

In order to reduce the total delay time and the storage, MDSC operator is proposed in [16]. The basic principle of this operator is similar to CDSC i.e., the test signal is delayed multiple times with various delay times such that the net sum of test signal and the delayed signals become zero. The delay times proposed in [16] are an integer multiple of $T/15$ such that delay time doesn't exceed fundamental time period T and thus, the operator is named as $MDSC_{15}$. The total delay time of $MDSC_{15}$ is always the maximum delay time i.e., $14T/15$ which is less than the delay time of $CDSC_{2,4,8,16}$. The operator $MDSC_{15}$ eliminates all harmonic frequency signals except $15k$ frequency signals when it is operated in dq frame. Hence, the $MDSC_{15}$ passes only $15k \pm 1$ frequency signals of abc frame. The lower order harmonics passed by $MDSC_{15}$ are 14 and 16 which are even, whereas in $CDSC_{2,4,8,16}$, they are odd i.e., 15 and 17. The bandwidth of SRF-PLL can be chosen high for $MDSC_{15}$ when compared to that of $CDSC_{2,4,8,16}$, since even harmonics are generally absent for power system applications. The dq equivalent of $MDSC_{15}$ operator are transformed on to $\alpha\beta$ frame using (8)

$$\begin{bmatrix} MDSC_{15}[v_{\alpha h}] \\ MDSC_{15}[v_{\beta h}] \end{bmatrix} = \begin{bmatrix} cos\ h^*\theta & -sin\ h^*\theta \\ sin\ h^*\theta & cos\ h^*\theta \end{bmatrix} \begin{bmatrix} MDSC_{15}[v_{dh}] \\ MDSC_{15}[v_{qh}] \end{bmatrix} \tag{8}$$

where,

$$MDSC_{15}[v_{dqh}] = \frac{1}{15}\sum_{l=0}^{14}\left[v_{dq}h(\omega t - Tl/15)\right].$$

The simplified expression of (8) is given in (9).

III. Performance Evaluation of Advanced PLLs

In order to evaluate the sole performance of DSOGI, $CDSC_{2,4,8,16}$ and $MDSC_{15}$ operators for various grid conditions, the similar bandwidth of SRF-PLLs are used for them. The performance evaluation of these advanced PLLs is carried out using MATLAB simulation. The accuracy of these advanced PLLs is decided based on the quality of frequency ω in SRF-PLL i.e., the steady-state error in phase angle extracted by PLL is zero for a ripple free frequency input to the integrator used in the SRF-PLL.

A. Frequency Jump

The frequency is increased to 52 Hz from 50 Hz at time $t = 0.4$ s, then it is decreased to 48 Hz at $t = 0.7$ s and then it shoots up to 100 Hz at $t = 1$ s as shown in Fig. 9(a). From frequency variation of PLLs, it is observed that for large jump in frequency, the steady-state tracking performance is good for all PLLs and the tracking speed of DSOGI-PLL is superior than other two PLLs. However, the tracking accuracy and speed of all PLLs are same for small change in frequency.

B. Voltage Unbalance

The unbalance in the fundamental voltage is observed in Fig. 9(b) from time $t = 0.4$ s to $t = 0.5$ s as well as from time $t = 0.8$ s to $t = 0.9$ s. The per unit voltages of phases a, b and c are respectively $1, 0.5$ and 0.8. From Fig. 9(b), it can be seen that there is no ripple in frequency for all three advanced PLLs and thus they have good phase angle tracking under fundamental unbalance condition.

C. Voltage Unbalance with Harmonics

The percentage of unbalance in fundamental voltage is considered same as in the previous case. In addition to this, $5^{th}, 7^{th}, 11^{th}$ and 13^{th} harmonics are added such that the THD of the resultant is about 27%. This is shown in Fig. 9(b) from time $t = 0.5$ s to $t = 0.6$ s. The ripple in frequency is seen only for DSOGI which leads to error in its phase angle tracking. Thus, performance of CDSC and MDSC is superior to DSOGI in the presence of harmonics.

D. Fundamental Balanced Voltage Sag

The fundamental balanced voltage sag is set for time $t = 0.6$ s to $t = 0.7$ s in Fig. 9(b). The phase angle tracking performance of all three PLLs are good for balanced sag in fundamental voltage as there is no ripple in frequencies.

E. Presence of DC Components

In general, grid voltages are sensed and processed in a controller for power electronic converter control. In this process, the dc components may be added to the sensed values. Therefore, in this case, performance of PLLs is evaluated for the presence of dc in the fundamental unbalanced voltages as shown in Fig. 9(b) from time $t = 0.7$ s to $t = 0.8$ s. The ripple in frequency is seen only for DSOGI which leads to error in its phase angle tracking. Thus, performance of CDSC and MDSC is superior to DSOGI in the presence of dc components.

$$\begin{bmatrix} DSC_n[v_{\alpha h}] \\ DSC_n[v_{\beta h}] \end{bmatrix} = \frac{1}{2}\begin{bmatrix} v_\alpha h(\omega t) + v_\alpha h(\omega t - \frac{T}{n})\cos\frac{2\pi h^*}{n} - v_\beta h(\omega t - \frac{T}{n})\sin\frac{2\pi h^*}{n} \\ v_\beta h(\omega t) + v_\beta h(\omega t - \frac{T}{n})\cos\frac{2\pi h^*}{n} + v_\alpha h(\omega t - \frac{T}{n})\sin\frac{2\pi h^*}{n} \end{bmatrix} \tag{7}$$

$$\begin{bmatrix} MDSC_{15}[v_{\alpha h}] \\ MDSC_{15}[v_{\beta h}] \end{bmatrix} = \frac{1}{15}\begin{bmatrix} v_\alpha h(\omega t) + \sum_{l=0}^{14}\left\{v_\alpha h(\omega t - \frac{Tl}{15})\cos\frac{2\pi h^* l}{15} - v_\beta h(\omega t - \frac{Tl}{15})\sin\frac{2\pi h^* l}{15}\right\} \\ v_\beta h(\omega t) + \sum_{l=0}^{14}\left\{v_\beta h(\omega t - \frac{Tl}{15})\cos\frac{2\pi h^* l}{15} + v_\alpha h(\omega t - \frac{Tl}{15})\sin\frac{2\pi h^* l}{15}\right\} \end{bmatrix} \tag{9}$$

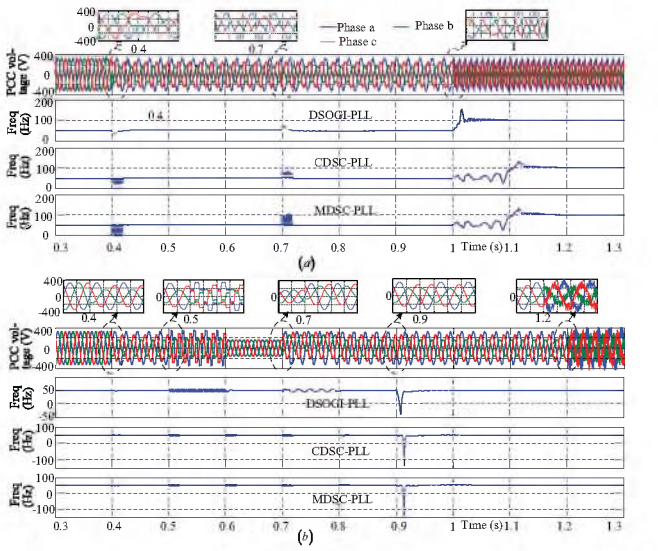

Fig. 9: Simulation results: Frequencies of advanced PLLs under (a) grid frequency variations (b) various other grid conditions.

F. Phase Angle Jump

The maximum jump in phase angle i.e., 180^0 is set at time $t = 0.9\,\mathrm{s}$ in Fig. 9(b). The peak-undershoot in frequency of DSOGI-PLL is less when compared to that of other two PLLs. However, there is no ripple in frequency of all PLLs at steady-state. Thus, the phase angle tracking performance is not affected by these PLLs under phase angle jump.

G. Distortions

The distorted unbalanced voltages are set for time $t = 1.2\,\mathrm{s}$ to $t = 1.3\,\mathrm{s}$ in Fig. 9(b). There is no effect seen on frequency due to distortions and thus the performance of all PLLs are satisfactory.

IV. Conclusion

This paper presents a comprehensive review on advanced PLLs such as SOGI, CDSC and MDSC based PLLs for an accurate extraction of FFPS components. The performance of PLLs are evaluated for various grid conditions using MATLAB simulation. All the harmonics are attenuated but not completely nullified by SOGI which results in unsatisfactory phase angle tracking performance for the presence of harmonics and dc components in grid voltages. The delay operators in CDSC and MDSC are chosen such that set of harmonics are completely eliminated, but it allows other harmonics without attenuation. Therefore, the performance of CDSC and MDSC based PLLs are well satisfactory for all grid conditions until grid has no dominant harmonics which can't be eliminated by them. From this, it is concluded that CDSC and MDSC based PLLs are most preferable than SOGI based PLL for islanded and grid connected microgrid applications.

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