Reactive Power Estimation based control of Self Supported Dynamic Voltage Restorer (DVR)

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***Abstract*--The dynamic voltage restorer (DVR) is an attractive solution to protect sensitive loads from voltage sag, swell, unbalance and voltage harmonics. When the injected voltages by the DVR are in quadrature with line currents, the DVR can be supported by a capacitor on DC side. In this paper, a new and simple control algorithm based on reactive power estimation is proposed for a self-supported DVR. The DVR is controlled by tracking the load voltages to their reference values computed by the proposed control algorithm in the stationary reference frame. Furthermore, a proportional-resonant (PR) controller is utilized to avoid any reference frame transformation. Moreover, the PR controller has very high gain at both positive and negative sequence frequencies and thus it is used to achieve a better unbalance compensation without using two separate positive and negative sequence controllers. The proposed control strategy is validated by performing simulation studies in MATLAB environment. The simulation results for voltage sag, swell, harmonic and unbalance compensation using the proposed control algorithm are discussed.**

***Index Terms*—**Dynamic voltage restorer, power quality, voltage sag, voltage swell, and voltage unbalance compensation.

I. Introduction

THE power quality (PQ) problems and solutions to these problems have gained much importance in recent years. The main causes for poor power quality are: extensive use of nonlinear loads in distribution system for efficient and controlled use of energy, integration of distributed generators based on the renewable power (such as, solar and wind) and the occurrence of frequent faults on the electrical network. Under the generic name of custom power devices [2] a new group of compensators like dynamic voltage restorer (DVR), the distribution static synchronous compensator (DSTATCOM) and unified power quality conditioner (UPQC) have been developed and used for improving power quality in the distribution system. Some of the critical loads like dairy food industry, chip manufacturing industry, large computer networks etc. are very sensitive to supply related power quality problems. Voltage sags, swells, transients, unbalance and harmonic distortion are major power quality problems in the supply voltage. These power quality problems can be effectively compensated using a DVR.

The DVR is a voltage source converter (VSC) based power electronics device connected in series between the supply and sensitive loads through a series transformer. It can protect sensitive loads from supply side voltage quality problems by injecting the compensating voltage into the distribution line. When the injected voltages by DVR are in quadrature with the feeder currents, it does not require any active power for compensation. A small amount of active power to overcome the DVR system losses however should be supported to achieve a self-supporting DC bus. The disadvantage of quadrature voltage injection is that in case of a voltage sag/swell event the restored voltage may not be in-phase with pre-sag/swell voltage and, the compensation range is highly dependent on load power factor [15].

The different topologies of DVR and its protection are discussed in [9-10]. The analysis, design and voltage injection schemes of a self-supported DVR are explained in the [2, 11]. In [11-24], different control strategies have been developed for the control of the DVR. Some of the popular techniques are: the instantaneous reactive power theory (IRPT) [4], synchronous reference frame theory (SRFT) [12, 24], adaline based fundamental extraction [13], instantaneous symmetrical component theory (ISCT) [14, 15], and space vector modulation [19].

The frequent unsymmetrical faults in the power system generally cause the unbalanced voltage sags. To compensate for such unbalanced voltage sags, DVR needs to inject compensating voltages with both positive and negative-sequence components. These can be achieved using two separate proportional-integral (PI) controllers, each for positive and negative-sequence voltages, in *d-q* synchronous frame [24]. The approach proposed in [24] is computationally intensive due to the transformation from stationary frame to synchronous frame and vice-versa.

In this paper, a new control algorithm is developed based on estimation of instantaneous load reactive power for generation of reference load voltages in the stationary reference frame. The load voltages are controlled to its reference values using PR controller in the stationary reference frame. A PR controller achieves good positive and negative-sequence fundamental voltage regulation simultaneously as it has high gains around both positive and negative-sequence fundamental frequencies [23]. Then implementation of DVR using VSC with PWM control is discussed in this paper. The extensive simulations are performed using MATLAB with its Simulink

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and Sim Power System (SPS) tool boxes for verifying the proposed control algorithm for DVR.

II. Proposed DVR Control Strategy Development

The main aim of the DVR is to inject compensating voltages in series with the supply for regulating the load terminal voltages. The schematic of the DVR connected power system is shown in Fig. 1, where the DVR is represented by ideal voltage sources (V_{Ca}, V_{Cb}, V_{Cc}).

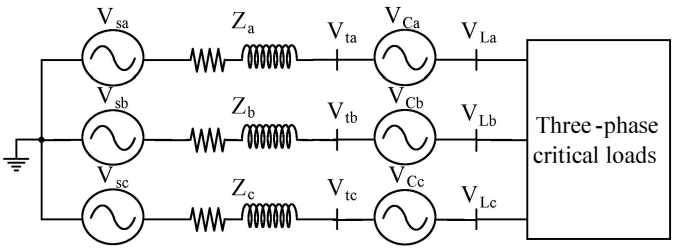

Fig. 1 Schematic diagram DVR connected power system.

The energy storage device is a capacitor and thus the DVR should not supply any real power in steady state. This implies that in steady state the phase angle difference between instantaneous DVR voltages and instantaneous line currents must be 90 degree.

A. *Reference Load voltage extraction under balanced sinusoidal supply condition*

By assuming balanced sinusoidal supply voltages and balanced load, from Fig.1

$$v_{tk} + v_{ck} = v_{Lk}^{*}; \qquad k = a, b, c \tag{1}$$

where v_{tk}, v_{ck} and v_{Lk}^{*} is the instantaneous terminal voltages, DVR voltages and reference load voltages, respectively. The instantaneous active power supplied by the source (p_S) can be calculated using the instantaneous terminal voltages (v_{ta}, v_{tb}, v_{tc}) and load currents (i_{La}, i_{Lb}, i_{Lc}) as,

$$p_S = v_{ta} i_{La} + v_{tb} i_{Lb} + v_{tc} i_{Lc} \tag{2}$$

Note that the calculated instantaneous active power p_S is constant in (2) since the terminal voltages and load currents are assumed to be balanced. Let V_{LL} (line to line) be the desired *rms* value of the load voltage. Since the load voltage will be regulated through quadrature voltage injection, the active power absorbed by load (p_L) is equal to active power supplied by source (p_S). Assuming that the load side voltage is regulated to V_{LL} by DVR, the total apparent power absorbed by the load can be computed as,

$$s_L = \sqrt{a} V_{LL} \tag{3}$$

where, $$a = i_{La}^2 + i_{Lb}^2 + i_{Lc}^2 \tag{4}$$

From (2) and (3), the reactive power absorbed by load can be estimated as,

$$q_L = \sqrt{a V_{LL}^2 - p_L^2} \tag{5}$$

The instantaneous reference load voltages are then computed using (2), (4) and (5) as,

$$\begin{bmatrix} v_{La}^{*} \\ v_{Lb}^{*} \\ v_{Lc}^{*} \end{bmatrix} = \frac{1}{\sqrt{3}a} \begin{bmatrix} \sqrt{3} p_L * i_{La} + q_L * (i_{Lc} - i_{Lb}) \\ \sqrt{3} p_L * i_{Lb} + q_L * (i_{La} - i_{Lc}) \\ \sqrt{3} p_L * i_{Lc} + q_L * (i_{Lb} - i_{La}) \end{bmatrix} \tag{6}$$

B. *Reference Load voltage extraction under unbalanced and/or distorted supply condition*

When the supply is unbalanced and/or distorted the algorithm discussed in the previous sub-section may not perform adequately to maintain balanced sinusoidal load voltages. The calculated instantaneous active power in (2) is no longer constant due to unbalanced and/or distorted terminal voltages.

For the algorithm to work under such situations, one needs to extract the instantaneous fundamental positive sequence component of terminal voltages from the unbalanced voltages. Let the unbalanced and distorted terminal voltages be given by,

$$v_{tk} = v_{tk1\_f} + v_{tk\_rest}; \qquad k = a, b, c \tag{7}$$

where v_{tk1_f} is the fundamental positive-sequence component of v_{tk} and v_{tk_rest} is the remaining portion containing the influence of unbalance and harmonics. The modification is thus to replace v_{ta}, v_{tb} and v_{tc} in (2) by v_{ta1_f}, v_{tb1_f} and v_{tc1_f} respectively.

$$p_S = v_{ta1\_f} i_{La} + v_{tb1\_f} i_{Lb} + v_{tc1\_f} i_{Lc} \tag{8}$$

To extract the steady state instantaneous fundamental positive sequence component of terminal voltages, the fundamental positive sequence extractor based on auxiliary active power computation is proposed and it is discussed in next sub-section.

C. *Fundamental positive sequence voltage extractor*

The block diagram of the proposed fundamental positive sequence extractor based on auxiliary active power computation is shown in Fig. 2. The auxiliary current unit vectors i_a, i_b and i_c are computed using the outputs of the PLL circuit; $\sin\theta$ and $\cos\theta$ as,

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \sin\theta \\ \cos\theta \end{bmatrix} \tag{9}$$

Note that i_a, i_b and i_c have a magnitude of unity and they are in phase with fundamental positive sequence terminal voltages. The unbalanced and distorted voltages v_{ta}, v_{tb} and v_{tc} are used together with auxiliary current unit vectors i_a, i_b and i_c to calculate the auxiliary active power p_{aux} as,

$$p_{aux} = v_{ta} i_a + v_{tb} i_b + v_{tc} i_c \tag{10}$$

When the input voltages are balanced sinusoidal then calculated auxiliary active power p_{aux} is constant but, when input voltages are unbalanced and/or distorted then auxiliary active power p_{aux} will compose of two parts. One of the parts will be a constant component containing the information about fundamental positive sequence terminal voltages and the second part will be varying component influenced by negative sequence terminal voltages and harmonics. To extract fundamental positive sequence voltages only constant component of p_{aux} is required. The constant part of the auxiliary active power p_{dc_aux} is extracted by passing p_{aux} through a low pass filter (LPF).

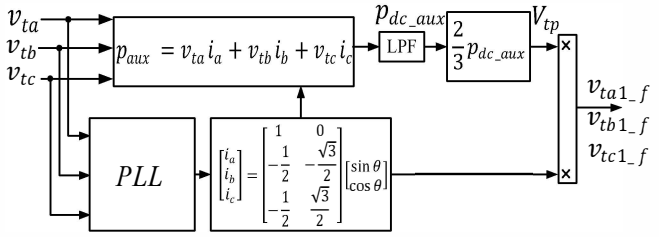

Fig. 2 Proposed fundamental positive sequence extractor

The fundamental positive sequence terminal voltage magnitude V_{tp} is then computed as,

$$V_{tp} = \frac{2}{3} p_{dc\_aux} \tag{11}$$

Using (9) and (11), the extracted fundamental positive sequence voltages are given by,

$$\begin{bmatrix} v_{ta1\_f} \\ v_{tb1\_f} \\ v_{tc1\_f} \end{bmatrix} = V_{tp} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{12}$$

III. DVR Power Circuit and Its Control

Fig. 3 shows the DVR circuit configuration along with a dc capacitor (C_{dc}) to maintain a self-supporting dc bus. The VSC is connected to the network through ripple filter (L_r, C_r, R_r) and injection transformer. The terminal voltages (V_{ta}, V_{tb}, V_{tc}) behind source impedances (Z_a, Z_b, Z_c) have power quality problems and the DVR injects voltages (V_{Ca}, V_{Cb}, V_{Cc}) through the injection transformer to get desired sinusoidal load voltages (V_{La}, V_{Lb}, V_{Lc}).

The proposed control scheme for the DVR is illustrated in Fig. 4. As shown, the terminal voltages are measured and processed through fundamental positive sequence extractor to extract fundamental positive sequence components of unbalanced and distorted terminal voltages. These extracted voltages are used along with measured load currents to calculate the instantaneous active power given by source as per (8). As practical DVR has losses in inverter, transformer and filter, it is required by the DVR to absorb a small amount of active power (p_{loss}) to self-support its DC bus against these losses. The instantaneous active power absorbed by load considering DVR losses can be written as,

$$p_L = p_S - p_{loss} \tag{13}$$

In (13) p_{loss} is estimated using a proportional-plus-integral (PI) controller over DC link voltage (v_{dc}).

$$p_{loss} = \left(k_p + \frac{k_i}{s}\right) e_{dc} \tag{14}$$

where, e_{dc} is the error between reference DC link voltage (v_{dc}^{ref}) and measured DC link voltage processed through LPF (v_{dc}^{f}).

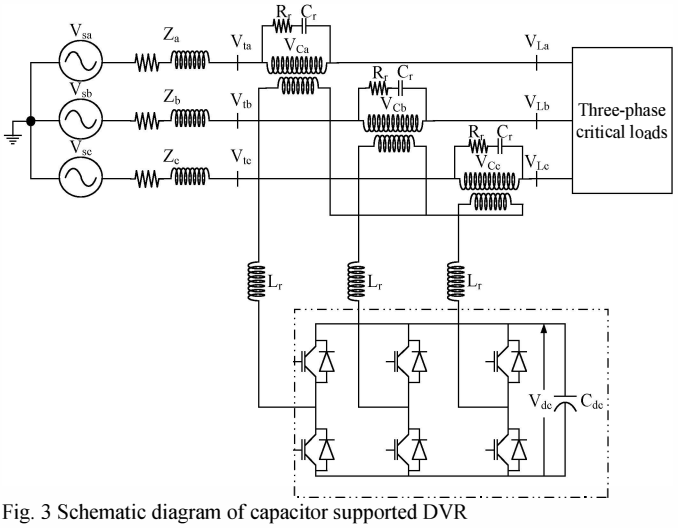

Fig. 3 Schematic diagram of capacitor supported DVR

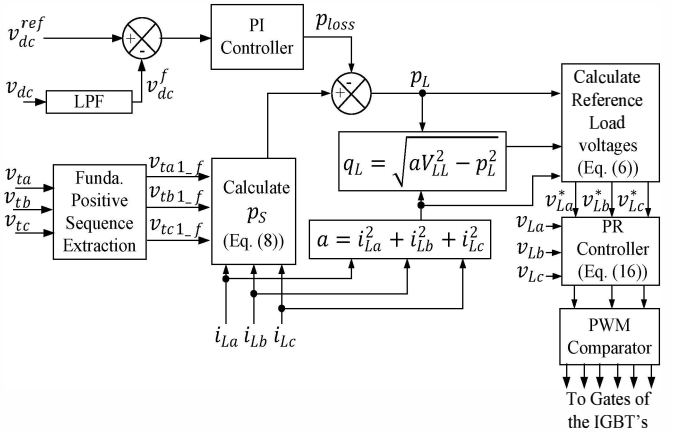

Fig. 4 The complete block diagram of proposed control algorithm.

The instantaneous reactive power absorbed by the load (q_L) is estimated using (5). Using (6) the reference load voltages (v_{La}^*, v_{Lb}^*, v_{Lc}^*) are calculated in stationary frame to avoid reference frame transformations. The VSC of DVR is controlled indirectly by tracking load voltages to their reference values (v_{La}^*, v_{Lb}^*, v_{Lc}^*) using the proportional plus resonant (PR) controllers in each phase.

The transfer function of ideal PR controller is given in (15) and it can be mathematically derived by transforming a d-q frame PI controller to the stationary frame without consideration of the redundant cross coupling terms [25]. The ideal PR controller has an infinite gain at selected resonant frequency ω_{res}, which can be set equal to angular fundamental frequency.

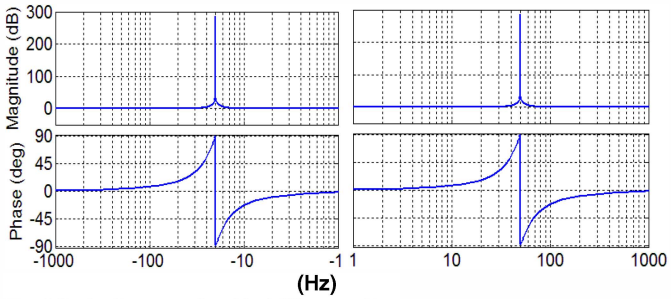

Fig. 5 Bode diagram of an ideal PR controller.

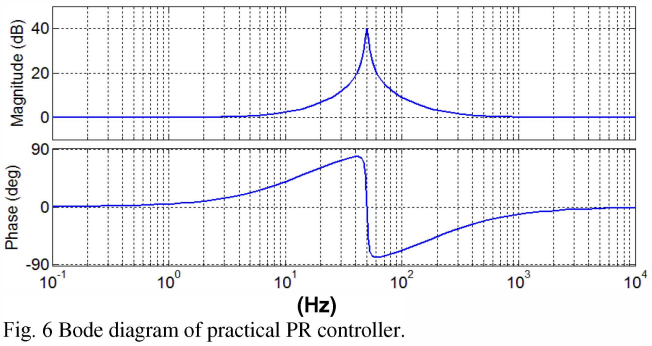

Fig. 6 Bode diagram of practical PR controller.

$$H(s) = k_p + \frac{2k_i s}{s^2+\omega_{res}^2} \tag{15}$$

In [26], it is shown that by transforming PI controllers of both positive and negative-sequence synchronous frames to the stationary frame, the transfer function of PR controller given in (15) can be obtained. Furthermore, if the same PI parameters are employed in both synchronous frames the cross coupling terms generated from positive and negative-sequence synchronous frames cancel each other. Therefore, the PR controller has infinite gains at both the positive and negative fundamental frequencies. In principle, only one PR controller will achieve zero steady state error for both positive- and negative-sequence regulation. A Bode plot of the ideal PR controller with k_p, k_i and ω_{res} equal to 1, 100 and 100π respectively is shown in Fig. 5. As stated it can be seen that the ideal PR controller has infinite gains at $\pm$50Hz. The ideal PR controller is tuned to one frequency so, there can be practical problems during its implementation particularly under the situation of frequency variations. More realistic form of PR controller with damping is therefore proposed in [26] and it is adopted in this work. The transfer function of practical PR controller with damping is given by,

$$H(s) = k_p + \frac{2k_i\omega_c s}{s^2+2\omega_c s+\omega_{res}^2} \tag{16}$$

where ω_c is the controller cutoff frequency. The Bode plot of (16) with k_p, k_i, ω_{res} and ω_c equal to 1, 100, 100π and 2π respectively is given in Fig. 6. It can be seen that the controller has a wider bandwidth around the resonant frequency. This reduces the sensitivity of controller to slight frequency variations, at the expense of a reduced resonant peak. However, the resulting resonant peak is still sufficient for fundamental tracking error elimination. It is important to consider the sampling and transport delay due to discretized implementation while selecting the controller parameters k_p, k_i, ω_{res} and ω_c. The details of the controller parameters tuning can be found in [23] and [27].

IV. Simulation Results

To validate the proposed control algorithm, test system with DVR was simulated in MATLAB. The performance of the DVR for different supply disturbances is evaluated under various operating conditions. The data of the simulated test system is given in the appendix. Figs. 7 to 10 give the simulation results for various conditions. In all the results quantities are shown in per unit (*p.u.*).

The performance of DVR controlled through the proposed control algorithm to compensate balanced voltage sag is shown in Fig. 7. The balanced voltage sag of 15% (for 5 cycles) in terminal voltage is introduced at 0.2 *s* (Fig. 7(a)). It can be seen that by injecting the necessary compensating voltages through DVR (Fig. 7(b)) the load voltage is regulated to its reference value 1 *p.u.* (Fig. 7(c)). The load currents and the magnitudes of terminal and load voltages are depicted in Fig. 7(d) and Fig. 7(e), respectively. There is a little reduction of DC link voltage at the beginning of the sag but, it is regulated to its reference value by DC link voltage regulator within two cycles of AC mains (Fig. 7(f)).

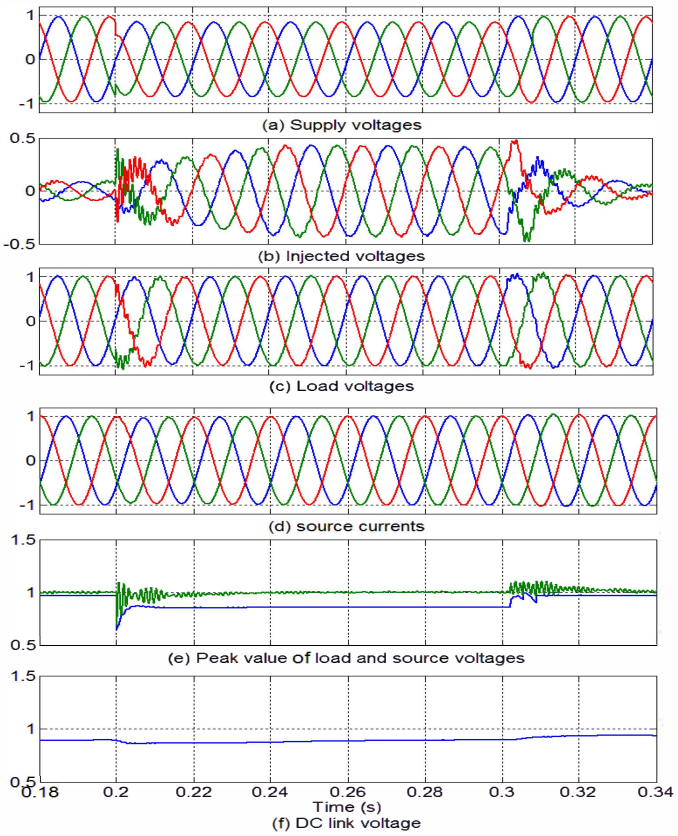

Fig.7. Compensation of balanced voltage sag using DVR.

Fig. 8 shows the performance of the proposed control algorithm to compensate voltage swell of 15%. As expected, the load voltages are regulated to 1 *p.u.* (Fig. 8(c)) by DVR and its performance is found to be satisfactory. The performance of DVR to compensate unbalanced voltage sag is illustrated in Fig. 9. An unbalanced sag in two phases of source voltage is introduced at 0.20 *s* (Fig. 9(a)). It can be seen

that the load voltage is regulated to its rated value (Fig. 9(c)) by injecting required amount of positive and negative-sequence voltages by DVR.

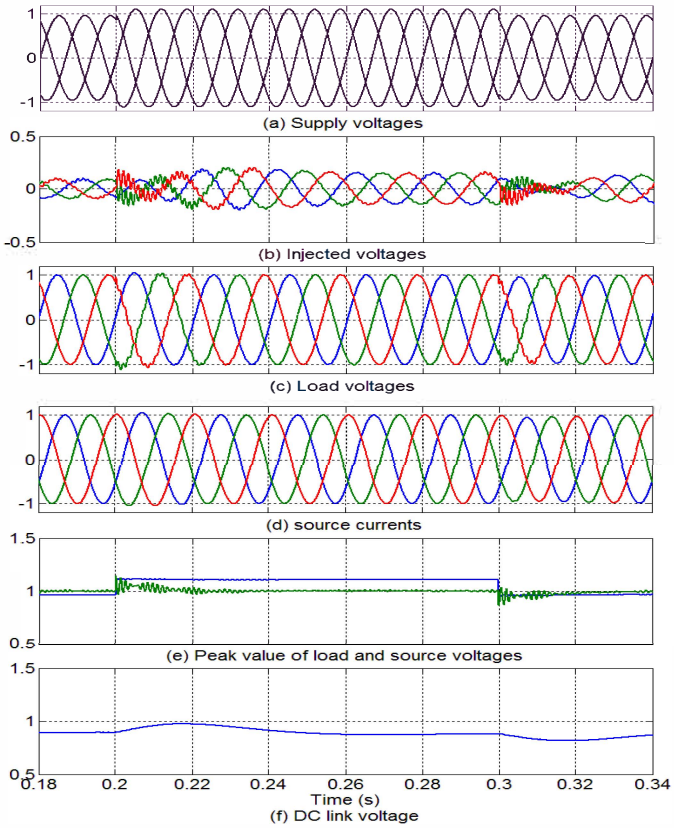

Fig.8 Compensation of balanced voltage swell using DVR.

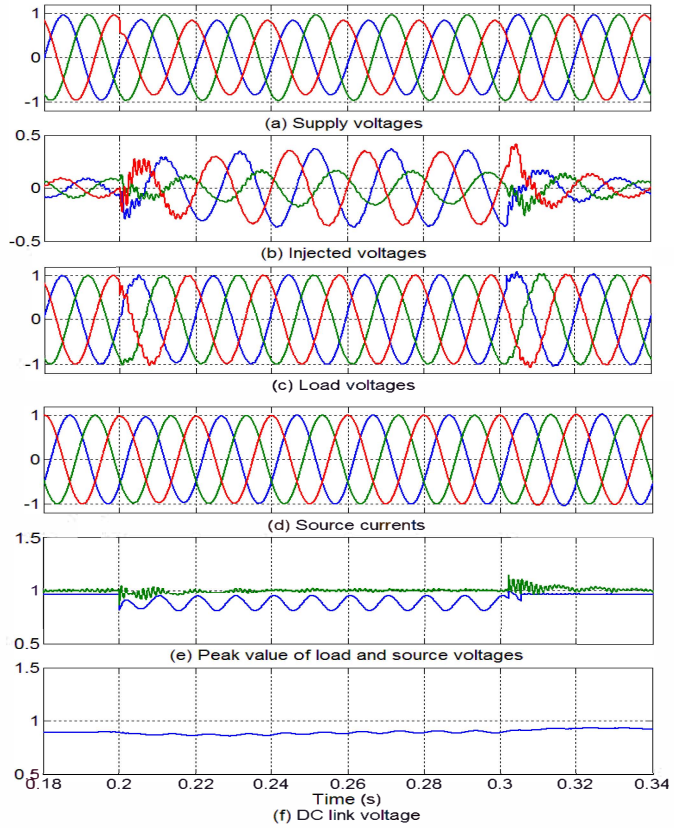

Fig.9 Compensation of unbalanced voltage sag using DVR.

It is worthy to note that accurate unbalanced voltage compensation is achieved using a single PR controller for each phase in stationary frame without any complex quantity transformation. The harmonics compensation in load voltage is achieved and depicted in Fig. 10. The terminal voltages are distorted by adding 5^{th} and 7^{th} harmonic of magnitude 10% and 7% respectively (Fig. 10(a)). The terminal voltages have a total harmonic distortion (THD) of 13%. After harmonic compensation by DVR, the load voltages have a THD of 3.35% (Fig. 10(c)). It should be noted here that the PR controller has a comparatively small gain at the frequency other than resonance frequency so, the load voltage waveforms cannot be achieved perfect sinusoidal. When expected distortion in terminal voltages is high or the application requires very low distortion in load voltages, selective harmonic compensation can be applied using extra resonant (R) controller for selected harmonic tuned to be resonate at the harmonic frequency [28].

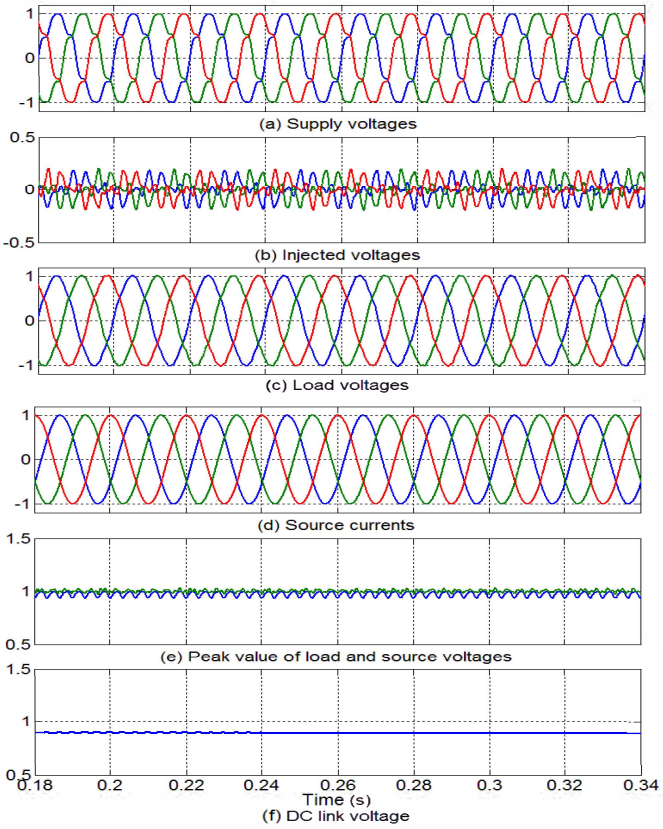

Fig.10 Compensation of harmonics using DVR

V. CONCLUSION

A simple control algorithm based on reactive power estimation is proposed for the generation of reference load voltages in stationary reference frame to control the DVR. Furthermore, a fundamental positive sequence extractor based on auxiliary active power computation is developed and discussed in this paper. The PR controller is used to track reference load voltages in stationary frame. It is shown that, single PR controller can achieve good positive and negative-sequence compensation simultaneously which eliminates the need of two separate positive and negative-sequence controllers. The proposed control algorithm of the DVR has

been validated and found satisfactory for the compensation of balanced sag/swell, unbalanced sag and harmonics in terminal voltages. It is also shown that the DVR is capable of providing self-supporting dc bus.

VI. APPENDIX

- Simulated test system parameters

Base voltage/power: 415 *V*/10 *kVA*
AC source voltage: 415 *V*, 50 *Hz*
Line Impedance: L_s= 3.5 *mH*, R_s=0.1 Ω
Loads: Linear- 10 *kVA*, 0.8 *pf* lag
DVR:
Ripple filter: L_r= 2 *mH*, C_r = 10 μF, R_r= 4.8 Ω
DC bus capacitance of DVR: 1000 μF
DC bus voltage of DVR: 300 *V*
PWM switching frequency: 10 *kHz*
Controller sampling frequency: 20 *kHz*
Series Injection Transformer: Three numbers of single-phase transformers of each of rating 3 *kVA*, 200 *V*/300

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