A Comparison of Control Algorithms for DSTATCOM

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***Abstract*—In this paper, a Distribution STATic COMpensator (DSTATCOM) is proposed for compensation of reactive power and unbalance caused by various loads in distribution system. An evaluation of three different methods is made to derive reference currents for a DSTATCOM. These methods are an instantaneous reactive power theory, a synchronous reference frame theory, and a new Adaline-based algorithm. The Adaline-based algorithm is an adaptive method for extracting reference current signals. These schemes are simulated under MATLAB environment using SIMULINK and PSB toolboxes. Simulation and experimental results demonstrate the performance of these schemes for the control of DSTATCOM.**

***Index Terms*—Adaline, Distribution STATic COMpensator (DSTATCOM), instantaneous reactive power (IRP) theory, load balancing, reactive power compensation, synchronous reference frame (SRF) theory.**

I. Introduction

IN PRESENT day distribution systems, major power consumption has been in reactive loads, such as fans, pumps, etc. These loads draw lagging power-factor currents and therefore give rise to reactive power burden in the distribution system. Moreover, situation worsens in the presence of unbalanced loads. Excessive reactive power demand increases feeder losses and reduces active power flow capability of the distribution system, whereas unbalancing affects the operation of transformers and generators [1]. A Distribution STATic COMpensator (DSTATCOM) can be used for compensation of reactive power and unbalance loading in the distribution system [2]. The performance of DSTATCOM depends on the control algorithm used for extraction of reference current components. For this purpose, many control schemes are reported in literature, and some of these are instantaneous reactive power (IRP) theory, instantaneous symmetrical components, synchronous reference frame (SRF) theory, current compensation using dc bus regulation, computation based on per phase basis, and scheme based on neural network techniques [3]–[11]. Among these control schemes, IRP and SRF theories are most widely used.

In this paper, a DSTATCOM is controlled using IRP and SRF theories for compensation of reactive power and unbalance, and these methods are compared with a new Adaline-based control algorithm. This Adaline-based control algorithm is simple and needs less computational efforts [12]–[14]. A fast adaptive linear element (Adaline)-based reference current estimator extracts real positive sequence current component without any phase shift. The estimation of reference currents through Adaline utilizes a least-mean squares (LMS) algorithm for the calculation of weights [13]. A MATLAB-based simulation study is presented for these three control techniques of DSTATCOM. Simulation results demonstrate the effectiveness of these three control algorithms of DSTATCOM for compensation of reactive power and unbalanced loading. Hardware of the DSTATCOM is also developed to validate Adaline-based control scheme with a self-supported dc bus using a dSPACE DS1104 R&D controller.

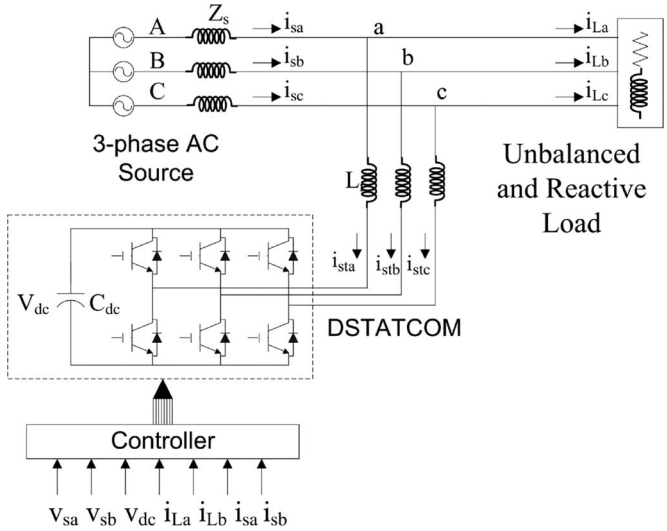

Fig. 1. Basic circuit diagram of the DSTATCOM system.

II. System Configuration

Fig. 1 shows the basic circuit diagram of a DSTATCOM system with lagging power-factor loads connected to a three-phase three-wire distribution system. Lagging power-factor load is realized by star-connected resistive–inductive (R–L) load. An unbalanced load is realized by disconnecting load from phase a using a circuit breaker. A three-phase voltage source converter (VSC) working as a DSTATCOM is realized using six insulated-gate bipolar transistors (IGBTs) with antiparallel diodes. At ac side, the interfacing inductors are used to filter high-frequency components of compensating currents.

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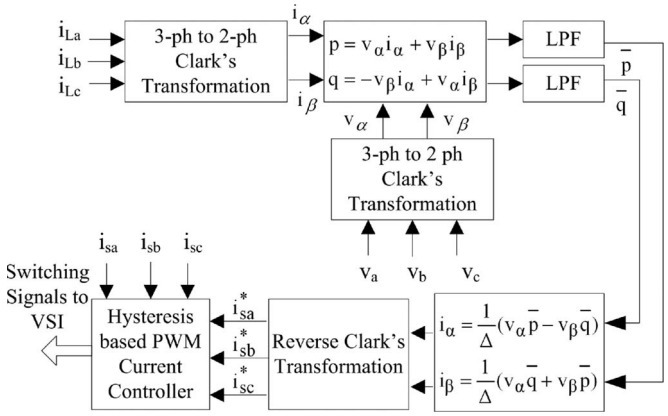


Fig. 2. Block diagram of the reference current extraction using IRP theory.

III. Control Algorithms

For reactive power compensation, a DSTATCOM provides reactive power as needed by the load, and therefore, the source current remains at unity power factor (UPF). Since only real power is being supplied by source, load balancing is achieved by making the source reference current balanced. Reference source current used to decide the switching of the DSTATCOM has real fundamental frequency component of the load current, which is being extracted by these techniques.

A. IRP Theory

IRP theory was initially proposed by Akagi [3]. This theory is based on the transformation of three-phase quantities to two-phase quantities in α–β frame and the calculation of instantaneous active and reactive power in this frame [3], [4]. A basic block diagram of this theory is shown in Fig. 2. Sensed inputs v_a, v_b, and v_c and i_{La}, i_{Lb}, and i_{Lc} are fed to the controller, and these quantities are processed to generate reference current commands (i^*_{sa}, i^*_{sb}, and i^*_{sc}), which are fed to a hysteresis-based pulsewidth modulated (PWM) signal generator (shown in Fig. 2) to generate final switching signals fed to the DSTATCOM; therefore, this block works as a controller for DSTATCOM shown in Fig. 1.

The system terminal voltages are given as

$$\begin{aligned} v_a &= V_{\rm m}\sin(\omega t) \\ v_b &= V_{\rm m}\sin(\omega t - 2\pi/3) \\ v_c &= V_{\rm m}\sin(\omega t - 4\pi/3) \end{aligned} \tag{1}$$

and the respective load currents are given as

$$\begin{aligned} i_{La} &= \sum I_{Lan}\sin\{n(\omega t) - \theta_{an}\} \\ i_{Lb} &= \sum I_{Lbn}\sin\{n(\omega t - 2\pi/3) - \theta_{bn}\} \\ i_{Lc} &= \sum I_{Lcn}\sin\{n(\omega t - 4\pi/3) - \theta_{cn}\}. \end{aligned} \tag{2}$$

In a–b–c coordinates, a, b, and c axes are fixed on the same plane, apart from each other by $2\pi/3$. The instantaneous space vectors v_a and i_{La} are set on the "a" axis, and their amplitude varies in positive and negative directions with time. This is true for the other two phases also. These phasors can be transformed into α–β coordinates using Clark's transformation as follows:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{3}$$

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{4}$$

where α and β axes are the orthogonal coordinates. Conventional instantaneous power for three-phase circuit can be defined as

$$p = v_\alpha i_\alpha + v_\beta i_\beta \tag{5}$$

where p is equal to conventional equation

$$p = v_a i_a + v_b i_b + v_c i_c. \tag{6}$$

Similarly, the IRP is defined as

$$q = -v_\beta i_\alpha + v_\alpha i_\beta. \tag{7}$$

Therefore, in matrix form, instantaneous real and reactive powers are given as

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} v_\alpha & v_\beta \\ -v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix}. \tag{8}$$

The α–β currents can be obtained as

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{1}{\Delta} \begin{bmatrix} v_\alpha & -v_\beta \\ v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} p \\ q \end{bmatrix} \tag{9}$$

where

$$\Delta = v_\alpha^2 + v_\beta^2. \tag{10}$$

Instantaneous active and reactive powers p and q can be decomposed into an average (dc) and an oscillatory component

$$\begin{aligned} p &= \overline{p} + \widetilde{p} \\ q &= \overline{q} + \widetilde{q} \end{aligned} \tag{11}$$

where $\overline{p}$ and $\overline{q}$ are the average (dc) part and $\widetilde{p}$ and $\widetilde{q}$ are the oscillatory (ac) part of these real and reactive instantaneous powers. Reference source currents are calculated to compensate the IRP and the oscillatory component of the instantaneous active power. In this case, the source transmits only the nonoscillating component of the active power. Therefore, the reference source currents $i^*_{s\alpha}$ and $i^*_{s\beta}$ in α–β coordinate are expressed as

$$\begin{bmatrix} i^*_{s\alpha} \\ i^*_{s\beta} \end{bmatrix} = \frac{1}{\Delta} \begin{bmatrix} v_\alpha & -v_\beta \\ v_\beta & v_\alpha \end{bmatrix} \begin{bmatrix} \overline{p} \\ 0 \end{bmatrix}. \tag{12}$$

These currents can be transformed in a–b–c quantities to find the reference currents in a–b–c coordinates using reverse

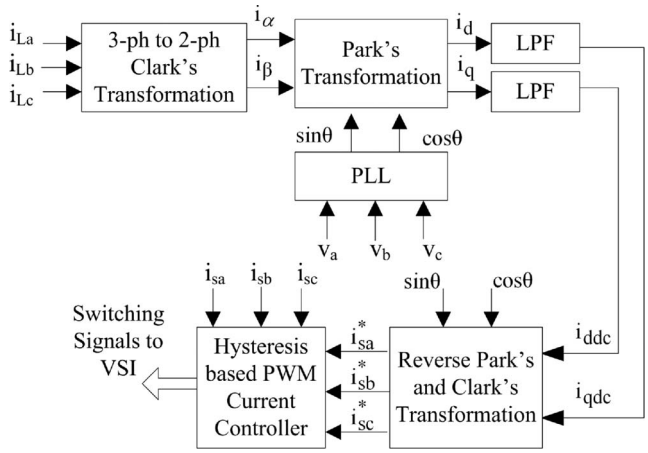


Fig. 3. Block diagram of the reference current extraction using SRF theory.

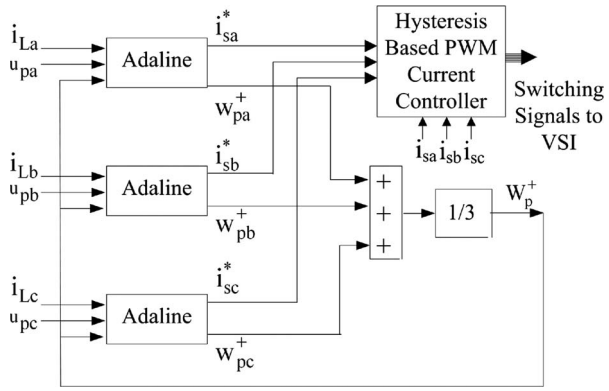


Fig. 4. Block diagram of the reference current extraction using Adaline-based theory.

Clark's transformation

$$\begin{bmatrix} i_{sa}^* \\ i_{sb}^* \\ i_{sc}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1 & 0 \\ 1/\sqrt{2} & -1/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_0^* \\ i_{s\alpha}^* \\ i_{s\beta}^* \end{bmatrix} \quad (13)$$

where i_0^* is the zero sequence component, which is zero in three-phase three-wire system.

B. SRF Method

SRF theory is based on the transformation of currents in synchronously rotating d–q frame [5], [6]. Fig. 3 shows the basic building blocks of this theory. Sensed inputs v_a, v_b, and v_c and i_{La}, i_{Lb}, and i_{Lc} are fed to the controller. Voltage signals are processed by a phase-locked loop (PLL) [15] to generate unit voltage templates (sine and cosine signals). Current signals are transformed to d–q frame, where these signals are filtered and transformed back to abc frame (i_{sa}, i_{sa}, and i_{sc}), which are fed to a hysteresis-based PWM signal generator [12] to generate final switching signals fed to the DSTATCOM; therefore, this block works as a controller for DSTATCOM shown in Fig. 1.

Similar to the p–q theory, current components in α–β coordinates are generated, and using θ as a transformation angle, these currents are transformed from α–β to d–q frame defined as (Park's transformation)

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix}. \quad (14)$$

SRF isolator extracts the dc component by low-pass filters (LPFs) for each i_d and i_q realized by moving averager at 100 Hz. The extracted dc components $i_{d\mathrm{dc}}$ and $i_{q\mathrm{dc}}$ are transformed back into α–β frame using reverse Park's transformation

$$\begin{bmatrix} i_{\alpha\mathrm{dc}} \\ i_{\beta\mathrm{dc}} \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_{d\mathrm{dc}} \\ i_{q\mathrm{dc}} \end{bmatrix}. \quad (15)$$

From these currents, the transformation is made to obtain three-phase reference source currents in a–b–c coordinates using (13). Reactive power compensation can also be provided by keeping i_q component zero for calculating the reference source currents.

C. Adaline-Based Control Algorithm

The basic theory of the proposed Adaline decomposer has been based on LMS algorithm and its training through Adaline, which tracks the unit vector templates to maintain minimum error. A block diagram of Adaline-based control scheme is shown in Fig. 4. The basic concept of theory used here can be understood by considering the analysis in single-phase system, which is given as under.

The supply voltage may be expressed as

$$v_s = V_1 \sin \omega t. \quad (16)$$

Sensed load current that is made up of active current (i_p^+), reactive current (i_q^+) for positive sequence, and negative sequence current (i^-) can be decomposed in parts as

$$i_L = i_p^+ + i_q^+ + i^-. \quad (17)$$

The control algorithm is based on the extraction of current component in phase with the unit voltage template. To estimate the fundamental frequency positive sequence real component of load current, the unit voltage template should be in phase with the system voltage and should have unit amplitude, and it must be undistorted. For the calculation of templates, voltage at the point of common coupling is sensed. Sensed voltages are filtered through a bandpass filter, and their amplitude is computed. Sensed three-phase voltages (as shown in Fig. 1) are divided by this amplitude to get three-phase voltage templates (u_a, u_b, and u_c shown in Fig. 4).

An initial estimate of the active part of current for single phase can be chosen as

$$i_p^+ = W_p \times u_p \quad (18)$$

where weight (W_p) is estimated using Adaline technique. The weight is variable and changes as per the load current and magnitude of phase voltage. This scheme for estimating weights corresponding to the fundamental frequency real component of current (for three-phase system), based on LMS-algorithm-tuned Adaline, tracks the unit voltage

templates to maintain minimum error $\{i_{L(k)} - W_{p(k)}u_{p(k)}\}$. The estimation of weight is given as per the following iterations [13]:

$$W_{p(k+1)} = W_{p(k)} + \eta \left\{ i_{L(k)} - W_{p(k)}u_{p(k)} \right\} u_{p(k)}. \tag{19}$$

The value of η (convergence coefficient) decides the rate of convergence and the accuracy of estimation. The practical range of convergence coefficient lies in between 0.1 and 1.0. Higher values of η provide fast convergence toward the final value but at the expense of some accuracy. The selected value of η here is considered as 0.2 to achieve high level of accuracy at the reasonable dynamic response. Three-phase reference source currents corresponding to positive sequence real component of load current may be computed as

$$i^*_{sa} = W^+_p u_{pa} \qquad i^*_{sb} = W^+_p u_{pb} \qquad i^*_{sc} = W^+_p u_{pc} \tag{20}$$

$$W^+_p = \left(W^+_{pa} + W^+_{pb} + W^+_{pc} \right) /3. \tag{21}$$

For the estimation of reference currents, weights are averaged to compute an equivalent weight for positive sequence current component in the decomposed form. The averaging of weights helps in removing the unbalance in the current components.

These three-phase reference source currents are fed to the hysteresis-based PWM current controller to control the source currents to follow the reference source currents in UPF mode of operation.

These currents are considered as the reference source currents $i_{\rm ref}$ $(i^*_{sa}, i^*_{sb},$ and $i^*_{sc})$, and along with the sensed source currents $i_{\rm act}$ $(i_{sa}, i_{sb},$ and $i_{sc})$, these currents are fed to a hysteresis-based PWM current controller to control the source currents to follow these reference currents. Switching signals generated by PWM current controller control the source currents close to the reference current. Switching signals are generated on the following logic, where hb is the hysteresis band around the reference current $i_{\rm ref}$.

1) If $(i_{\rm act}) > (i_{\rm ref} + hb)$, the upper switch of the leg is ON, and the lower switch is OFF.
2) If $(i_{\rm act}) < (i_{\rm ref} - hb)$, the upper switch of the leg is OFF, and the lower switch is ON.

This current control results in the control of the slow varying source current (as compared to DSTATCOM currents) and therefore requires less computational efforts. Moreover, this scheme automatically compensates the computational delay caused by the processor.

D. PI Controller for Maintaining Constant DC Bus Voltage of DSTATCOM

The operation of DSTATCOM system requires ac mains to supply real power needed to the load and some losses (switching losses of devices, losses in reactor, and dielectric losses of dc bus capacitor) in the DSTATCOM. Therefore, the reference source current, used to decide switching of DSTATCOM, has two components: One is the real fundamental frequency component of the load current, which is being extracted using

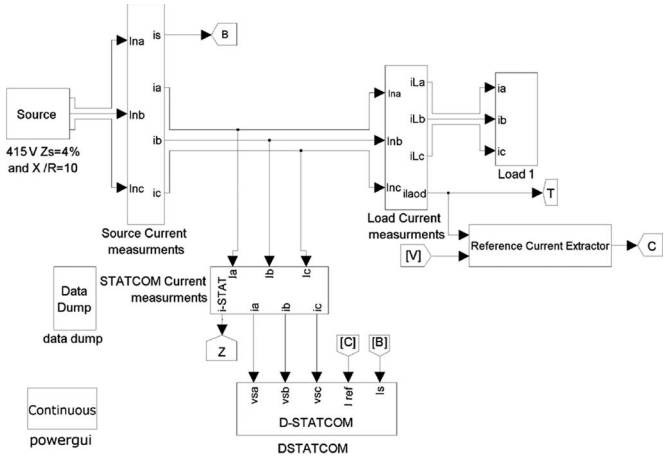


Fig. 5. MATLAB-based model of DSTATCOM system.

the p–q theory, SRF theory, or Adaline technique, and another component, which corresponds to the losses in DSTATCOM, is estimated using a proportional–integral (PI) controller over the dc bus voltage of the DSTATCOM.

To compute the second component of the reference active current, a reference dc bus voltage $(v^*_{\rm dc})$ is compared with the sensed dc bus voltage $(v_{\rm dc})$ of DSTATCOM. A comparison of the sensed dc bus voltage to the reference dc bus voltage of VSC results in a voltage error, which, in the nth sampling instant, is expressed as

$$v_{{\rm dc}l(n)} = v^*_{{\rm dc}(n)} - v_{{\rm dc}(n)}. \tag{22}$$

This error signal $v_{{\rm dc}l(n)}$ is processed in a PI controller, and the output $\{I_{p(n)}\}$ at the nth sampling instant is expressed as

$$I_{p(n)} = I_{p(n-1)} + K_{p{\rm dc}} \left\{ v_{{\rm dc}l(n)} - v_{{\rm dc}l(n-1)} \right\} + K_{i{\rm dc}} v_{{\rm dc}l(n)} \tag{23}$$

where $K_{p{\rm dc}}$ and $K_{i{\rm dc}}$ are the proportional and integral gains of the PI controller.

The output of this PI controller accounts for the losses in DSTATCOM, and it is considered as the loss component of the current. This component $(I_{p(n)})$ can be added with the average real power for controlling DSTATCOM by p–q theory. If the control is facilitated by SRF theory, the output of PI regulator can be added with d-axis component of the current signal. For controlling DSTATCOM by Adaline, the output of PI controller is added with the equivalent source currents.

IV. MATLAB-Based Model of DSTATCOM System

Fig. 5 shows the basic simulation model of DSTATCOM system that correlates to the system configuration shown in Fig. 1 in terms of source, load, DSTATCOM, and control blocks. The considered load is a combination of resistance and inductance connected in series for each phase. The load is star connected with a rating of 32 kVA at 0.8 pf. This DSTATCOM model is simulated with the above described p–q, SRF, and Adaline-based theories. Fig. 6(a)–(c) shows the simulation models for these theories that are inconsistent with the control

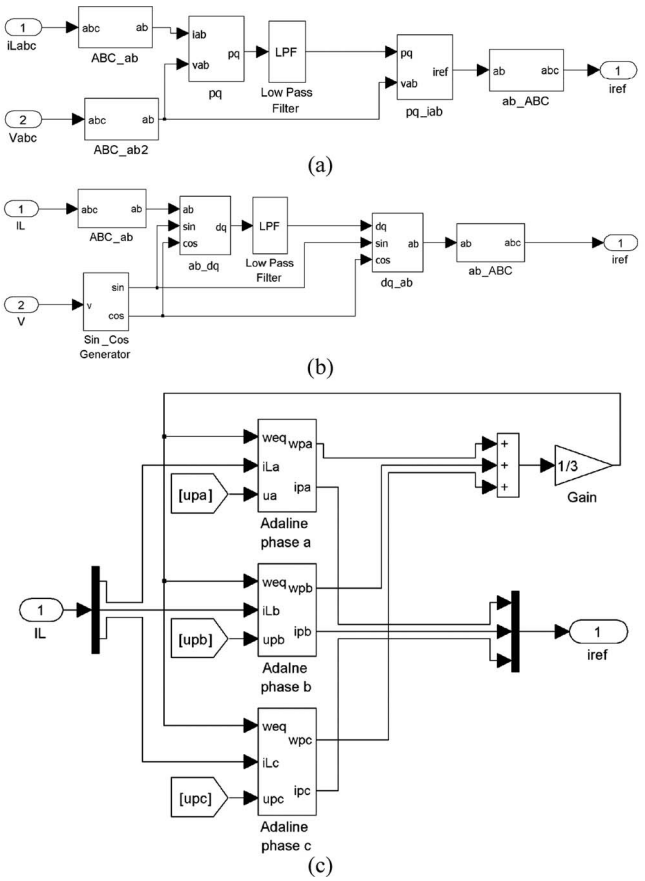


Fig. 6. MATLAB-based model of current extraction using (a) IRP, (b) SRF, and (c) Adaline-based theories.

schemes shown in Figs. 2–4. The model is assembled using the mathematical blocks of SIMULINK block set. Simulation is carried out in continuous mode at a maximum step size of 1×10^{-6} with ode15s (stiff/NDF) solver.

V. Results and Discussion

The performance of DSTATCOM is studied for all three methods of control techniques, and the following observations are made based on these results.

A. Control of DSTATCOM by IRP Theory

Fig. 7 shows the dynamic performance of a DSTATCOM using the IRP-theory-based current extractor. The considered load is resistive–reactive at 0.8 lagging power factor. The load has been increased from 16 to 32 kVA at 0.12 s, and unbalance is introduced at 0.18 s. After 0.24 s, the dynamics are shown in reverse sequence. A delay in compensation can be seen from source current waveforms. This delay is due to the LPF used for filtering power signals. Moreover, IRP theory uses voltage signals to compute instantaneous active and reactive powers; any distortion and unbalance in voltage will lead to the inaccurate calculation of reference source currents, which should contain only real fundamental frequency component of the load current.

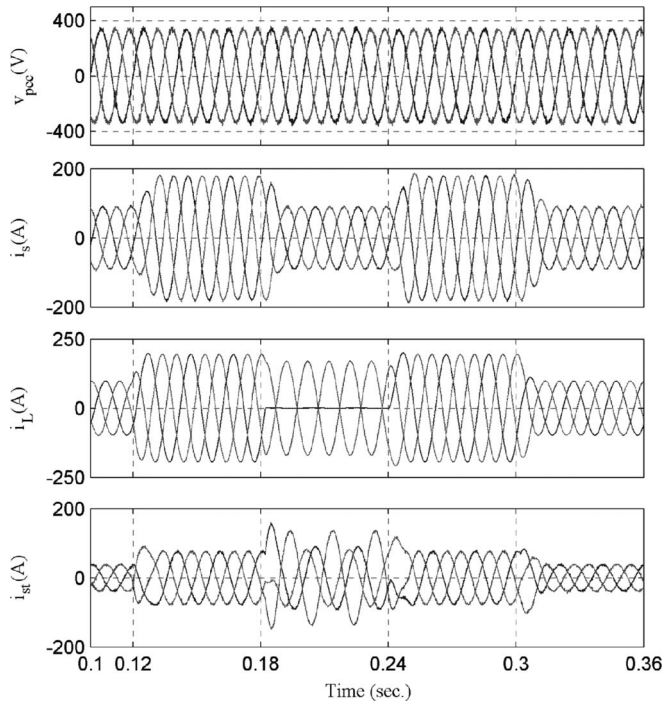


Fig. 7. Dynamic performance of a DSTATCOM controlled using IRP theory.

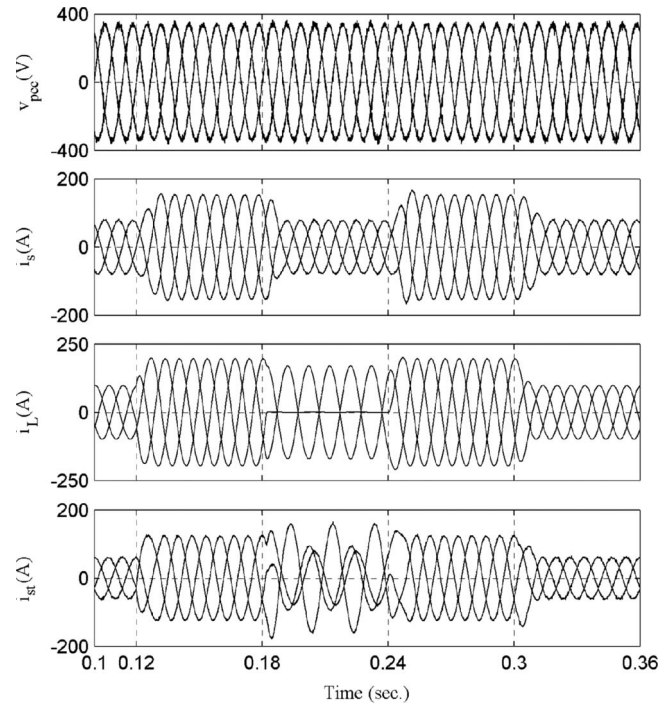


Fig. 8. Dynamic performance of a DSTATCOM controlled using SRF theory.

B. Control of DSTATCOM by SRF Theory

Fig. 8 shows the performance of a DSTATCOM controlled by SRF theory. Simulation is carried out for similar load changes and unbalanced conditions as of the previous case. The effect of delay due to LPF used for filtering signals in d–q frame can be seen in the extracted reference current waveform. The generation of voltage templates (sine and cosine) plays an important role in the calculation of reference source currents.

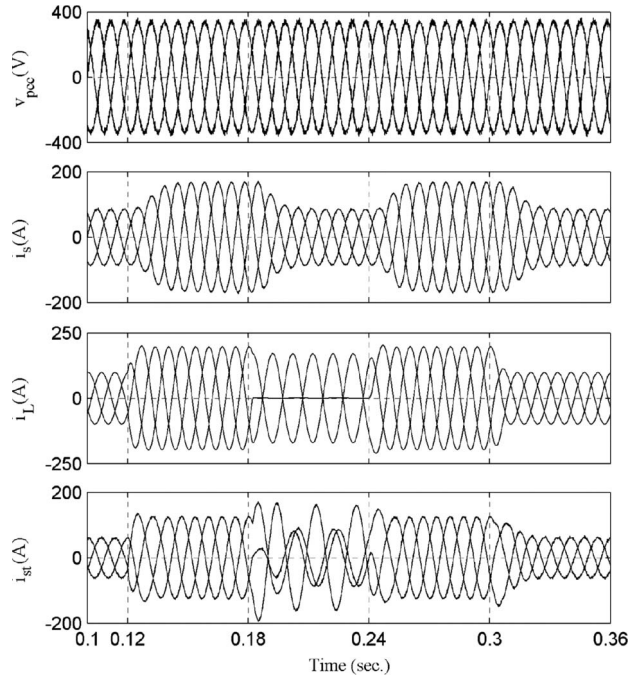


Fig. 9. Dynamic performance of a DSTATCOM controlled using Adaline-based current extractor.

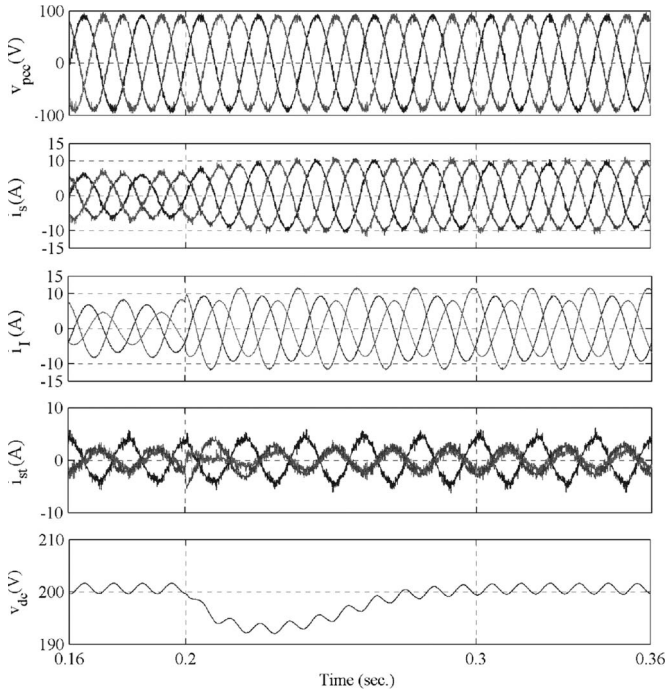


Fig. 10. Dynamic performance of a DSTATCOM with self-supporting dc bus controlled using Adaline-based current extractor.

These templates are generated using PLL, and therefore, the tuning of PLL is crucial. The operation of PLL is slow, and it also imposes some amount of delay in computation.

C. Control of DSTATCOM by Adaline-Based Algorithm

The performance of DSTATCOM is shown in Fig. 9, using Adaline technique. It can be observed that DSTATCOM with Adaline technique is able to meet the load changes within one cycle of sine wave. An advantage of the Adaline-based extractor is that it requires less computational efforts, and therefore, the implementation of this technique is much simpler. Moreover, there is an inherent linearity in Adaline, which makes it a fast technique. The speed of convergence can be varied by varying the value of η (convergence coefficient).

The operation of DSTATCOM with self-supporting dc bus is shown in Fig. 10. Its dc-bus voltage $(v_{\rm dc})$ is maintained at 200 V. The effect of a load change at $t = 0.2$ s can be seen on the dc bus voltage. Three-phase load currents corresponding to

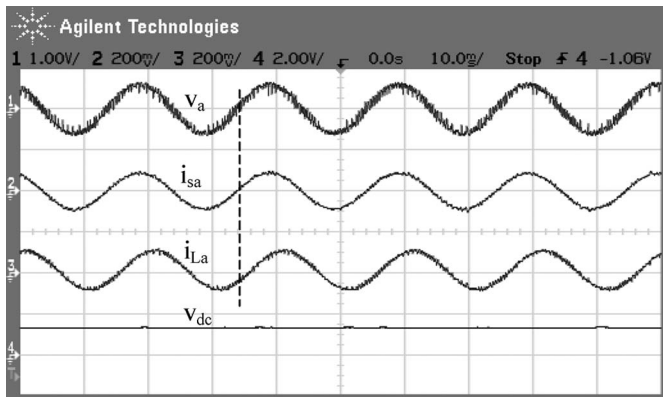


Fig. 11. Recorded waveforms of a-phase voltage, source, load currents, and dc bus voltage of DSTATCOM with unbalanced load (scales: 150 V/div for channel 1, 20 A/div for channels 2 and 3, and 300 V/div for channel 4).

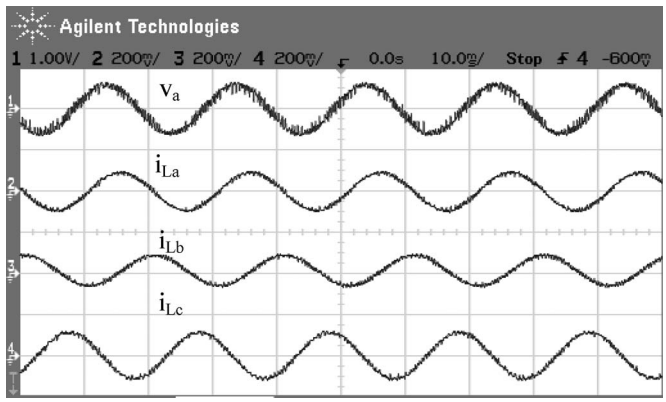


Fig. 12. Recorded waveforms of a-phase voltage and three-phase load currents (scales: 150 V/div for channel 1 and 20 A/div for channels 2, 3, and 4).

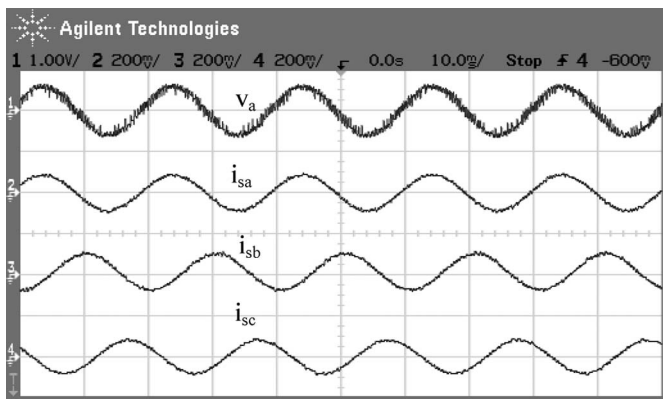
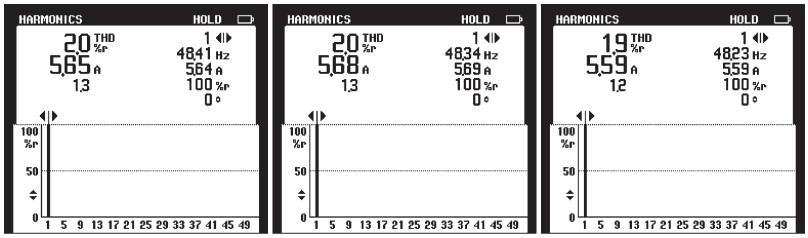


Fig. 13. Recorded waveforms of a-phase voltage and three-phase source currents (scales: 150 V/div for channel 1 and 20 A/div for channels 2, 3, and 4).



(a) (b) (c)

Fig. 14. Harmonic spectra of (a) a-, (b) b-, and (c) c-phase source currents.

a, b, and c phases are increased from 4.76, 3.17, and 5.90 A to 6.53, 5.61, and 8.12 A, respectively. The three-phase source currents are well balanced at 4.3, 4.25, and 4.33 A for light load condition and 6.50, 6.45, and 6.51 A under increased load condition for a, b, and c phases, respectively. Furthermore, some second harmonic oscillations in the dc bus voltage are observed in case of unbalancing of the load. The action of PI controller is observed to maintain the dc-bus voltage of DTATCOM at the reference value within a couple of cycles of ac sine wave.

D. Experimental Results

A hardware implementation of an Adaline-based control scheme of the DSTATCOM system is realized using dSPACE DSP processor. Two-phase load currents (i_{La} and i_{Lb}) and source currents (i_{sa} and i_{sb}) are sensed using Hall effect current sensors (LEM CT-100S). Three voltage sensors (LEM CV3-1500) are used to sense phase-a, phase-b, and dc link voltages. The software implementation of control algorithm is realized in MATLAB blocks in DSP dSPACE to generate the switching signals for IGBTs of DSTATCOM. These switching signals are fed to SKHI 22B drivers, which finally provide the gate voltage at the gate terminal of IGBT module (SKM 100GB128DN). For implementation, the control algorithm is run at a fixed step size of 78.125 μs. Interfacing filter inductor value is chosen to be 3 mH, and the value of dc bus capacitor is kept at 1650 μF.

The Adaline-based control scheme of the DSTATCOM is tested at unbalanced lagging power-factor load. The selected load is a three-phase star-connected resistive load with a three-phase star-connected inductive load connected in parallel to each other. The line–line voltage is kept at 110 V (rms), and the dc bus is maintained at 200 V. Three-phase load currents are unbalanced with values of 5.03, 6.04, and 7.76 A in a, b, and c phases, respectively. The compensation of this load is achieved using DSTATCOM with self-supporting dc bus. Fig. 11 shows the performance of DSTATCOM through the waveforms of a-phase voltage, source current, load current, and dc bus voltage. It can be clearly observed from this figure that the compensation for reactive power is provided by the DSTATCOM. Fig. 12 shows the a-phase voltage and three-phase unbalance load currents. Fig. 13 shows the a-phase voltage and three-phase source currents. The amplitude of a, b, and c phase currents are 5.65, 5.68, and 5.59 A, respectively. The harmonic spectra of three-phase source currents are shown in Fig. 14. The total harmonic distortion (THD) of a, b, and c phase source currents are 2%, 2%, and 1.9%, respectively. The THD of source currents is well below the limit of 5% prescribed

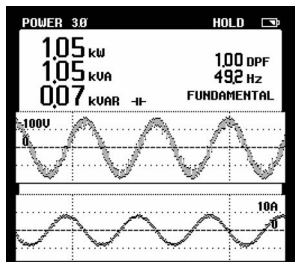


Fig. 15. Recorded three-phase power supplied by the source, showing line–line voltage (V_{ab}) and c-phase current.

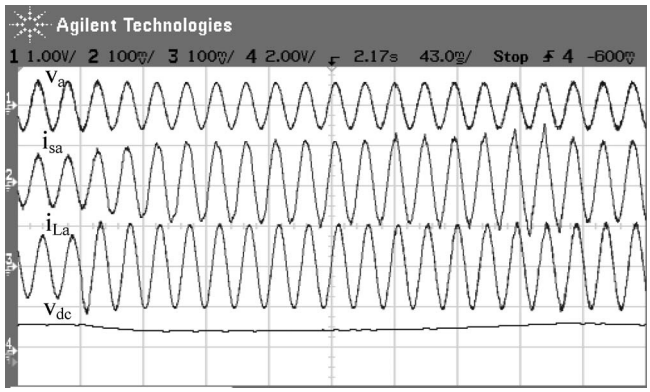


Fig. 16. Dynamic performance of DSTATCOM under load change (scales: 150 V/div for channel 1, 10 A/div for channels 2 and 3, and 300 V/div for channel 4).

in IEEE519 standard. The measured active and reactive power is shown in Fig. 15, which depicts that the source currents are at UPF and negligible reactive power is consumed from the source. These figures depict that the source currents are balanced and consist of only real fundamental frequency part of load currents. The dynamic performance of DSTATCOM is shown in Fig. 16 with a step change in the load. a-phase voltage, source current, load current, and dc bus voltage are shown in the figure. A phase load current is changed from 4.76 to 6.53 A. A three-phase load current change is in accordance with the simulation results shown in Fig. 10. It may be observed from this figure that the self-supporting dc bus of DSTATCOM is achieved for the satisfactory dynamic performance of the system.

VI. Conclusion

IRP and SRF theories and Adaline technique have demonstrated the satisfactory behavior of DSTATCOM. An Adaline-based control technique has resulted in considerable improved

performance of the DSTATCOM. The Adaline-based technique utilizes LMS algorithm to calculate the weights, and these calculations are performed online; therefore, this algorithm is able to extract the reference source currents in varying load conditions, which is not possible with other neural-network-based current extraction techniques. Simulated and test results have verified the effectiveness of these control algorithms.

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